Organic Complementary D Flip-Flops Enabled by Perylene Diimides and Pentacene

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***Abstract*—The development of organic complementary circuits has been largely limited by the development of suitable organic n-channel transistors. However, recent advances have led to materials such as the high-mobility air-stable n-channel organic semiconductor, N, N'-bis(n-octyl)-dicyanoperylene-3, 4 : 9, 10-bis (dicarboximide), PDI-8CN$_2$. Here, the fabrication of an organic complementary D flip-flop using PDI-8CN$_2$ n-channel transistors and pentacene p-channel transistors is described. The measured clock-to-output delay is 25 μs for 1 kHz, and 14 μs at the clock frequency of 5 kHz. This is the fastest clock speed for an organic complementary circuit yet achieved.**

***Index Terms*—Complementary circuits, D flip-flop, n-channel semiconductors, organic transistors, pentacene, perylene diimides.**

I. INTRODUCTION

ORGANIC field-effect transistors (OFETs) have a significant potential for use in a wide range of inexpensive and high-volume applications, such as radio-frequency identification tags, electronic paper, display driving electronics, and sensors [1], [2]. The development of organic transistor-based circuits has been limited to p-channel organic circuits, because of the paucity of environmentally robust high-performance n-channel organic semiconductors [3]–[5]. The lack of appropriate n-type materials is primarily due to the instability of the n-type charge carriers in most organic semiconductors, particularly upon exposure to a moisture and/or oxygen. Hence, the discovery and implementation of environmentally stable high-mobility n-channel organic transistors have been crucial for the fabrication of fast and reliable organic CMOS circuits.

One of the most promising families of n-type organic materials are the electron-deficient perylene-based and N-fluoroalkyl functionalized naphthalene-based semiconductors, which display good electrical properties and general air stability [6]. Among the n-type semiconductors investigated, appropriately functionalized perylene diimide (PDI)-based semiconductors have demonstrated a great promise due to their extremely high carrier mobility and significant air stability [7], [8]. N, N'-bis(n-octyl)-dicyanoperylene-3, 4 : 9, 10-bis (dicarboximide) (PDI-8CN$_2$) is a PDI derivative, where cyanation stabilizes charge carriers by lowering the energies of the lowest unoccupied molecular orbitals associated with an electron transport [7].

Organic CMOS clocked circuits, which are based on organic transistors, have been reported [9]. However, the maximum clock rate was only 1 kHz [10]. We have recently investigated the effect of an electrode/dielectric surface treatment along with implementing PDI-8CN$_2$ and demonstrated the potential of PDI-8CN$_2$ in organic CMOS ring oscillators with pentacene as p-type materials [11].

In this letter, we report the results of the electrical characterization in ambient atmosphere of bottom-contact transistors fabricated with both PDI-8CN$_2$ and pentacene. An organic semiconductor-based CMOS D flip-flop with PDI-8CN$_2$ and pentacene has also been fabricated and characterized. We report a clock rate of 5 kHz, which is the highest speed that any organic transistor-based complementary clocked circuit has achieved to date.

II. DEVICE FABRICATION AND CHARACTERISTICS

The bottom-contact structures of the discrete OFETs fabricated on silicon substrates with aluminum interconnect metal and double-gate dielectric layers, consisting of 200 nm of silicon nitride and 100 nm of silicon oxide, are shown in Fig. 1(a). These were fabricated in similar fashion as previously reported [10]. The channel width (W) and channel length (L) of the individual transistors are 2.0 mm and 7.5 μm, respectively. The use of self-assembled monolayers (SAM) in organic devices passivates the hydrophilic inorganic substrate with a lower surface energy monolayer [12], [13]. Likewise, alkanethiols were used to modify the surface energy of the gold electrodes to facilitate a charge-carrier injection. Thus, prior to the semiconductor deposition, samples were treated with hexamethyldisilazane (HMDS) vapor to functionalize the oxide-based substrate/dielectric, followed by 1-hexadecanethiol (HDT) vapor to functionalize the gold electrodes.

The PDI-8CN$_2$ was purified by multiple recrystallizations and thermally deposited onto a 100 °C substrate to a thickness of 42 nm. Pentacene films (42 nm) were deposited on the discrete FETs at a substrate temperature of 60 °C. The

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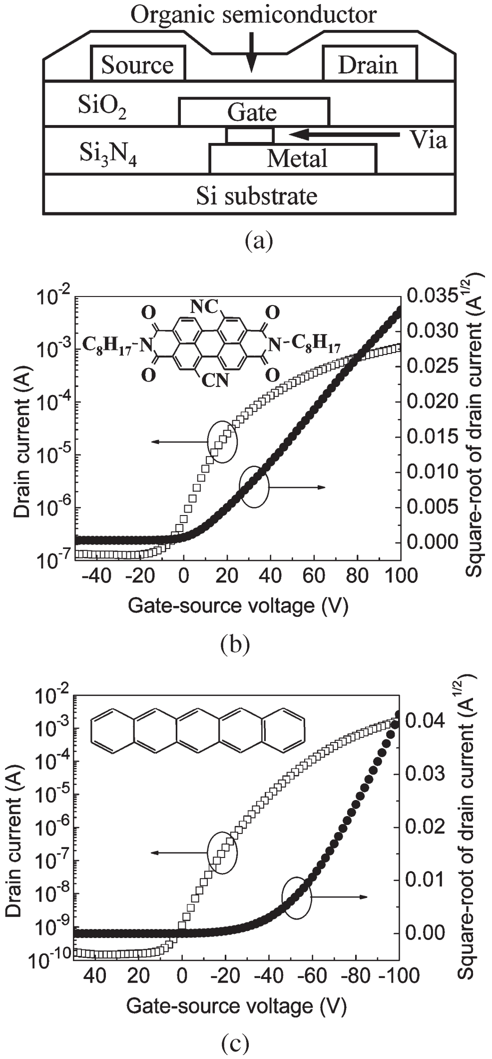

(a)

(b)

(c)

Fig. 1. (a) Structure of a bottom-contact OFET device. (b) Transfer characteristics of PDI-$8CN_2$ OFETs. The inset shows the chemical structure of PDI-$8CN_2$. (c) Transfer characteristics of pentacene OFETs. The inset shows the chemical structure of pentacene.

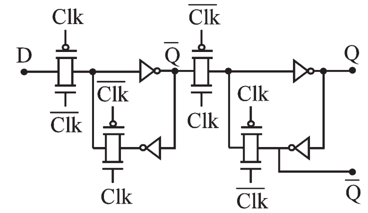

Fig. 2. Schematic diagram of a conventional D flip-flop.

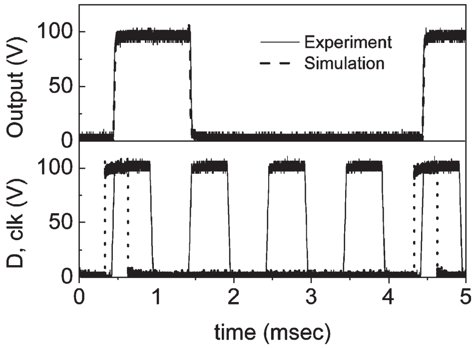

Fig. 3. Measured (solid line) and simulated (dotted line) output characteristics for the organic CMOS D flip-flop at 1 kHz. Dotted line shows the input data pulse.

base pressure was 4×10^{-7} torr and the deposition rate was 0.2–0.7 Å/s for these depositions. All electrical characterization was conducted in ambient atmosphere at room temperature. In the case of the complementary organic D flip-flop, the surface treatments and the deposition conditions used were the same as those used in the fabrication of the discrete transistors. The transfer characteristics of discrete bottom-contact PDI-$8CN_2$ and pentacene transistors, which are treated with both HMDS and HDT, are shown in Fig. 1(b) and (c), respectively, and the insets depict the chemical structures of PDI-$8CN_2$ and pentacene. For PDI-$8CN_2$ transistors, the field-effect mobility calculated in the saturation regime was 6.3×10^{-2} $\mathrm{cm}^2/\mathrm{Vs}$ at a source-drain voltage of 100 V, where $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio ($V_{\mathrm{DS}} = 100$ V) was 8.7×10^3, and the threshold voltage was 9.8 V. Most n-channel OFETs exhibit an electrical property degradation in ambient atmosphere; however, the mobility of PDI-$8CN_2$ in the saturation regime is comparable to the mobility obtained in vacuum, as reported previously in [11]. For pentacene transistors, the field-effect mobility calculated in the saturation regime was 0.29 $\mathrm{cm}^2/\mathrm{Vs}$ at a source-drain voltage of -100 V, where $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio ($V_{\mathrm{DS}} = -100$ V) was 1.1×10^7.

III. CIRCUIT DESCRIPTION

The D flip-flop is a basic storage element to construct sequential logic circuits and systems. A conventional master-slave D flip-flop schematic diagram is illustrated in Fig. 2. The pass-transistor logic-based D flip-flop requires 16 transistors, which is less than the transistors required for NOR/NAND-based logic. The D flip-flop is usually composed of two latches. Each latch consists of two CMOS transmission gates and two inverters. When the clock (Clk) is low, the input data D passes directly to the node −Q located at the end of the master latch. Since the clock bar is high at the same time, node −Q, which is located at the end of the master latch, is separated from the output node Q, and the feedback loop is closed so that the slave latch is in the storage state. The input data are sent to the slave latch when the clock is high. Therefore, the output starts to collect at the node Q when the input data D is at logic 1, and the clock converts from logic 0 to 1.

The measured and simulated characteristics for a pass-transistor logic-based D flip-flop at a clock frequency of 1 kHz are shown in Fig. 3. The solid line and dashed line represent the measured output and simulated output, respectively. PDI-$8CN_2$ and pentacene are used for the n-channel OFETs and the p-channel OFETs, respectively. All FETs in the D flip-flop have the same dimensions, channel width(W) = 2 mm and channel length (L) = 7.5 μm. The speed of this D flip-flop is limited by one transmission gate and one inverter delay after the clock switches from logic 0 to 1. The propagation (clock-to-output) delay for the slave D latch is about 25 μs. The D flip-flop fabricated was simulated using the T-SPICE

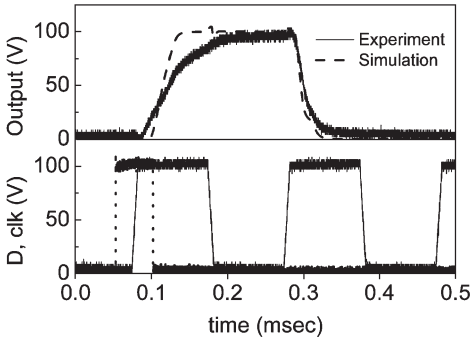

Fig. 4. Measured (solid line) and simulated (dotted line) output characteristics for the organic CMOS D flip-flop at 5 kHz. Dotted line shows the input data pulse.

program, using models and procedures similar to that described in [10]. The simulated clock-to-output delay is about 24 μs. Fig. 4 shows the measured and simulated characteristics for the same D flip-flop at a clock frequency of 5 kHz. The clock-to-output delays in measurement and simulation are decreased to 14 μs and 20 μs, respectively. It can be seen that the proposed circuit can operate correctly within reasonable error ranges caused by the simplicity of the model.

IV. CONCLUSION

We demonstrated here that PDI-8CN$_2$ is a very promising air-stable n-type organic semiconductor for use in organic-based complementary circuits. A complementary D flip-flop using PDI-8CN$_2$ and pentacene has been fabricated. The measured clock-to-output delay was 25 μs for 1 kHz and 14 μs at a clock frequency of 5 kHz, which agrees well with the SPICE simulation. This clock rate is the highest achieved so far for an organic complementary circuit.

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