

Variable Temperature Mobility Analysis of n-Channel, p-Channel, and Ambipolar Organic Field-Effect Transistors

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The temperature dependence of field-effect transistor (FET) mobility is analyzed for a series of n-channel, p-channel, and ambipolar organic semiconductor-based FETs selected for varied semiconductor structural and device characteristics. The materials (and dominant carrier type) studied are 5,5'''-bis(perfluorophenacyl)-2,2':5',2'':5'',2'''-quaterthiophene (1, n-channel), 5,5'''-bis(perfluorohexyl carbonyl)-2,2':5',2'':5'',2'''-quaterthiophene (2, n-channel), pentacene (3, p-channel); 5,5'''-bis(hexylcarbonyl)-2,2':5',2'':5'',2'''-quaterthiophene (4, ambipolar), 5,5'''-bis-(phenacyl)-2,2':5',2'':5'',2'''-quaterthiophene (5, p-channel), 2,7-bis((5-perfluorophenacyl)thiophen-2-yl)-9,10-phenanthrenequinone (6, n-channel), and poly(*N*-(2-octylododecyl)-2,2'-bithiophene-3,3'-dicarboximide) (7, n-channel). Fits of the effective field-effect mobility (μ_{eff}) data assuming a discrete trap energy within a multiple trapping and release (MTR) model reveal low activation energies (E_{A} s) for high-mobility semiconductors 1–3 of 21, 22, and 30 meV, respectively. Higher E_{A} values of 40–70 meV are exhibited by 4–7-derived FETs having lower mobilities (μ_{eff}). Analysis of these data reveals little correlation between the conduction state energy level and E_{A} , while there is an inverse relationship between E_{A} and μ_{eff} . The first variable-temperature study of an ambipolar organic FET reveals that although n-channel behavior exhibits $E_{\text{A}} = 27$ meV, the p-channel regime exhibits significantly more trapping with $E_{\text{A}} = 250$ meV. Interestingly, calculated free carrier mobilities (μ_0) are in the range of $\sim 0.2\text{--}0.8\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ in this materials set, largely independent of μ_{eff} . This indicates that in the absence of charge traps, the inherent magnitude of carrier mobility is comparable for each of these materials. Finally, the effect of temperature on threshold voltage (V_{T}) reveals two distinct trapping regimes, with the change in trapped charge exhibiting a striking correlation with room temperature μ_{eff} . The observation that E_{A} is independent of conduction state energy, and that changes in trapped charge with temperature correlate with room temperature μ_{eff} , support the applicability of trap-limited mobility models such as a MTR mechanism to this materials set.

1. Introduction

Advances in high-performance organic electronic devices have been primarily stimulated by the discovery of new materials, the development of novel processing/fabrication techniques, and advances in charge transport theories. Many applications have been enabled by advances in organic field-effect transistors (OFETs), including organic light-emitting technologies,^[1–4] organic TFT-driven active-matrix display backplanes (TFT = thin film transistor),^[5–7] ring-oscillators,^[8] diodes,^[9] and inverters.^[10–11] Even though new organic device technologies benefit from efficient FET operation, the community is still seeking a comprehensive understanding of OFET charge transport. Understanding the mechanism governing such phenomena involves fundamental questions of long-range and interfacial charge transport in organic solids and should facilitate the enlightened design/optimization of materials and devices.^[12–20]

The importance of understanding charge transport phenomena in OFETs has been highlighted by recent discoveries. Separate studies by de Leeuw et al.,^[21] Katz et al.,^[22] and Frisbie and co-workers^[23] argue that the ambient instability of n-channel FET operation for most organic semiconductors is the result of mobile electron trapping by ambient H₂O and/or O₂. These ideas were recently tested further, refined, and implemented to develop intrinsically air-stable n-channel FET semiconductors not relying on an O₂ barrier.^[24,25]

Further work demonstrated that rigorous exclusion of trapping species at the dielectric–semiconductor interface (e.g., hydroxyl groups)^[20d] can enable n-channel FET performance for both p-type and n-type semiconductors under inert atmosphere by eliminating deep electron traps with densities of $>10^{13}\text{ cm}^{-2}$. While these energetically deep, high-density charge traps must be overcome for efficient FET operation, it has been postulated that in most OFETs, shallow lower-density

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($\sim 10^{10}$ – 10^{12} cm $^{-2}$) traps limit the effective FET carrier mobility (μ_{eff}) for both p- and n-channel FET operation.^[15,23,26–28] Recent studies on single-crystal-based transistors also shed additional light on fundamental charge transport phenomena,^[29] and the interplay between carrier mobility and the gate dielectric permittivity has been investigated both in thin-film and single-crystal devices.^[29,30]

Variable-temperature studies of FETs have been used to characterize charge transport mechanisms, and generally reveal thermally activated charge transport, with activation energies (E_A) on the order of tens to hundreds of millielectronvolts. The most widely accepted model for charge transport in organic semiconductors involves multiple trapping and release (MTR).^[28] This model postulates that free carrier mobility (μ_0) is diminished by recurrent charge carrier trapping and thermal release from shallow trap states below the conduction band edge, defining the observed μ_{eff} . Since μ_{eff} is dominated by this trapping and release behavior, the density of these traps (N_{T0} , cm $^{-2}$) and their energy distribution in the band tail then determines the temperature dependence of μ_{eff} . For simplicity when modeling μ_{eff} , a discrete

trap state is typically assumed at energy E_T , which captures mobile charge according to Fermi–Dirac statistics. The density of trapped charge (N_T) in units of cm $^{-2}$ is therefore given by Equation 1 where E_F is the Fermi energy, k is the Boltzmann constant, and T is temperature.^[23,26,28]

$$N_T = N_{T0} \exp\left(\frac{-|E_T - E_F|}{kT}\right) \quad (1)$$

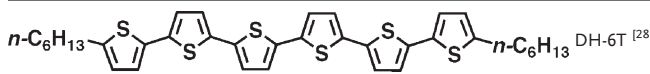
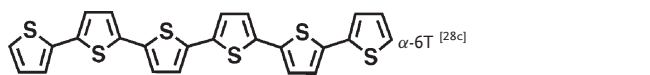
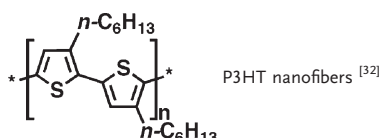
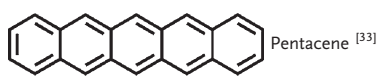
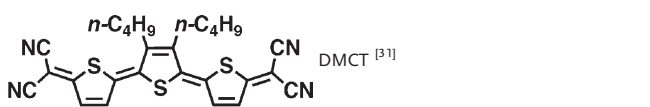
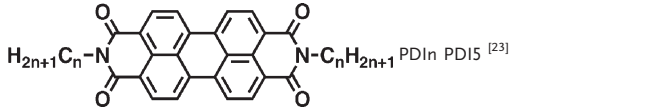
Using this single-energy-level trap model, μ_{eff} is given by Equation 2, where the activation energy E_A is the energy difference between the trap state and the conduction band edge.^[23,26–28,31,32]

$$\mu_{\text{eff}} = \mu_0 \exp\left(\frac{-E_A}{kT}\right) \quad (2)$$

This interpretation of the MTR mechanism predicts Arrhenius behavior for μ_{eff} and has been used to model mobility temperature dependence in both p-channel and n-channel FETs.^[11–13]

The variable-temperature behavior of p-channel semiconductors generally exhibits thermally activated μ_{eff} with behavior

Table 1. Summary of previous results of variable-temperature thin-film-based OFET behavior fit to an Arrhenius relationship.

Semiconductor [reference]	Carrier type	μ_{eff} [cm 2 V $^{-1}$ s $^{-1}$]	E_A [meV]	$\sim \Delta V_T$ [a] [mV]
 DH-6T ^[28b]	p	0.04	220	
 α -6T ^[28c]	p	0.15	~ 100	–16
α -6T ^[35]	p	0.02	~ 100	
 P3HT nanofibers ^[32]	p	0.06	65	–30
P3HT ^[27]	p	0.7	29	
P3HT ^[27]	p	0.092	85	
 Pentacene ^[33]	p	0.3	38	
Pentacene ^[34]	p	0.3	36	
Pentacene ^[36]	p	0.3	42	
Pentacene ^[36]	p	0.3	40	
 DMCT ^[31]	n	0.11	35	40
 PDI/PDI5 ^[23]	n	0.066	83	
PDI12 ^[26]	n	0.55	44	11
PDI5 ^[26]	n	0.39	91	15
PDI8 ^[26]	n	1.05	50	12

[a] Difference in threshold voltage (V_T) between $T = 300$ and ~ 80 K estimated from published plots.

consistent with the Arrhenius relationship of Equation 2 (Table 1). Pentacene-based FETs having $\mu_{\text{eff}} \approx 0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ typically exhibit $E_{\text{A}} = 39(3) \text{ meV}$,^[15,33,34] although one report^[33] reveals that devices with exceptionally high-room-temperature $\mu_{\text{eff}} = 1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ exhibit temperature-independent behavior. Sexithiophene-based (6T) p-channel FETs exhibit similar activated behavior with $E_{\text{A}} \approx 100\text{--}220 \text{ meV}$ for devices with $\mu_{\text{eff}} \approx 0.02\text{--}0.15 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[28,35] In separate work, the E_{A} of poly-3-hexylthiophene-based FETs (P3HT) was found to be 85 meV for devices with $\mu_{\text{eff}} = 0.092 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 29 meV for $\mu_{\text{eff}} = 0.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[27]

Several studies have recently noted negative OFET threshold voltage shifts with decreasing temperature and suggested that this may be a result of charge trapping. However, only a limited number of materials and experimental conditions were investigated in each of these studies, so that no general trends could be discerned.^[28,32,37] While some studies report consistent variable-temperature behavior once the materials processing aspects of FET fabrication are optimized, others report varying behavior for the same material, both within and between studies (Table 1). Two reports find that E_{A} is a strong function of the gate dielectric, substrate preparation, or other undefined parameters.^[15,33] The results from these studies suggest that the factors limiting charge transport are correlated with dielectric–semiconductor interfacial effects and/or semiconductor film microstructure.

More recently, n-channel dicyanomethylene-terthiophene (DCMT)- and perylene-diimide (PDI)-based FETs were found to exhibit Arrhenius-like temperature-activated behavior (Table 1). DCMT exhibits $E_{\text{A}} = 35(10) \text{ meV}$ for $\mu_{\text{eff}} \approx 0.12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (estimated from the Arrhenius plot) and an onset voltage shift of $\sim +40 \text{ V}$ from room temperature to 80 K.^[31] PDI derivatives exhibit $E_{\text{A}} \approx 60\text{--}90 \text{ meV}$ for devices having $\mu_{\text{eff}} \approx 0.07\text{--}1.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and also exhibit a positive onset voltage shift of $\sim 10\text{--}15 \text{ V}$.^[23,26] Since the dominant trapping mechanism for mobile electrons is thought to be different from that of holes,^[16,19–21] it is interesting that an MTR model (assuming discrete energy level traps) can satisfactorily fit both n- and p-channel variable-temperature μ_{eff} data.

The work summarized above demonstrates the utility of MTR to model variable-temperature FET response for several families of semiconductors. An analysis of fit parameters between studies and even within a single study reveals that μ_{eff} and E_{A} can vary dramatically, depending upon device fabrication parameters, such as dielectric composition, dielectric surface treatment, semiconductor deposition parameters, and source/drain electrode work function. Unfortunately, the marked sensitivity of E_{A} to these variations in experimental parameters prohibits close comparisons of materials between studies and has limited the clear definition of trends in charge transport mechanisms involving different semiconductors. Additionally, each report has typically focused on a single oligomer/polymer or family of molecules with only solubilizing group variations. Given the central role of trapping predicted by MTR and emphasized by recent discoveries of dramatic gate dielectric surface chemical and semiconductor frontier molecular orbital (MO) energy effects,^[19,20,38] significant insights should be possible from the ability to compare the variable-temperature behavior of FETs based on a diverse set of semiconductors, with materials processing, FET fabrication, and measurements performed under identical conditions with identical instrumentation.

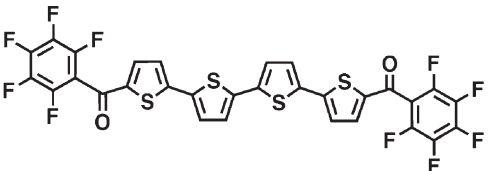
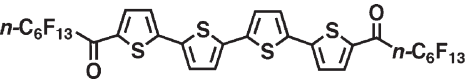
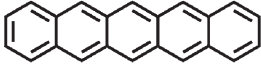
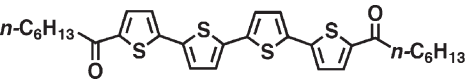
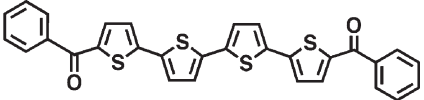
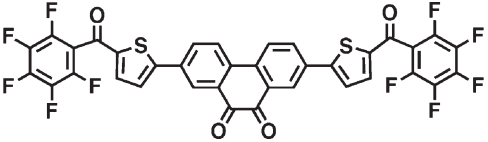
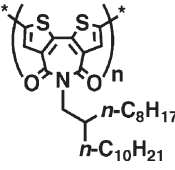
This contribution reports a detailed investigation of correlations between practical OFET device performance and fundamental charge transport parameters, such as E_{A} and the temperature dependence of trapped charge density (N_{T}) for semiconductor 1–7-based FETs, fabricated in parallel under optimized conditions (see Table 2 for structures of 1–7). These seven semiconductors were deliberately chosen to have different chemical and electronic structures, and were selected to probe the relationship of charge carrier trapping, conduction state energies, majority charge carrier type, room-temperature μ_{eff} , and V_{T} . Materials 1–6 are discrete oligomers having varying π -core composition and ancillary substitution with the lowest unoccupied molecular orbital (LUMO) energy levels of n-channel materials varying over a $\sim 0.6 \text{ eV}$ range. The diverse FET behaviors of 1–7-based FETs include electron, hole, or ambipolar mobilities between ~ 0.01 and $0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Semiconductor 7 is one of the first n-channel FET polymers to be prepared, exhibiting very substantial crystallinity and high $\mu_{\text{eff}} = 0.011 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. All devices are fabricated under their individual optimized semiconductor film growth conditions with identical substrate preparation, contact electrodes, characterization instrumentation, and FET measurement parameters.

A general inverse correlation between μ_{eff} and E_{A} is revealed here in this series of n-channel, p-channel, and ambipolar materials. Additionally, the calculated values of μ_0 are surprisingly found to be very similar for all members of the series, even though the magnitude of μ_{eff} varies by $\sim 10^2 \times$ and the charge carrier sign changes across materials series 1–6. The relationship of conduction state energy to shallow trapping events modeled by MTR is studied here for the first time in OFETs, and reveals minimal correlation. Rather, these findings suggest that mobility-limiting shallow traps are not directly dependent upon the semiconductor conduction band energy. Finally, this study reveals a clear and intriguing relationship between V_{T} shift, trap density, MO/conduction state energies, and μ_{eff} .

2. Results and Discussion

The thermally activated OFET behavior for all compounds investigated will first be presented. Fits of the μ_{eff} data assuming a discrete trap energy MTR model (Eq. 2) will then be shown to reveal Arrhenius-like behavior and that E_{A} scales inversely with room-temperature μ_{eff} values. For each semiconductor, a minimum of ten devices was measured at each temperature to improve precision, yielding standard deviations below 15%. Interestingly, the derived E_{A} parameters are found to be independent of conduction state energy or carrier type, suggesting that hole and electron carriers encounter comparable trap distributions irrespective of the conduction band energy and carrier charge. Next, calculated μ_0 values are discussed and found to be largely independent of μ_{eff} . Finally, the effect of temperature on V_{T} will be analyzed (in combination with room-temperature subthreshold swing measurements) to calculate N_{T} as a function of temperature, revealing a striking correlation between ΔN_{T} and μ_{eff} . These results are discussed in the context of previous observations, found to be consistent, and contribute considerably to understanding OFET charge transport phenomena.

Table 2. Semiconductors, their FET properties, and first redox potential (reduction for n-channel materials and oxidation for p-channel materials) studied in this work.

Semiconductor	Carrier Type	μ_{eff} [cm ² V ⁻¹ s ⁻¹]	V_T [V]	$E_{\text{redox}}^{1/2}$ [V vs. SCE]
	n	0.4	+28	-1.05
	n	0.3	+36	-0.88
	p	0.39	-10	+0.48 ^[39,40]
	n (p)	0.1 (0.01)	+42 (-60)	-1.06
	p	0.04	-49	-0.95
	n	0.02	+25	-0.45
	n	0.011	+67	-1.11

2.1. Thermal Activation of the Mobility

Plots of μ_{eff} versus $1000/T$ reveal Arrhenius-like behavior and negligible deviations from linearity (Fig. 1a). Attempts to plot μ_{eff} versus $T^{0.5}$ to fit a delocalized charge transport model or versus $T^{0.25}$ to fit a variable-range hopping model, exhibit poor adherence to these models and substantial error in their linear least-squares fits when compared to Arrhenius plot fits. Linear fits to the Arrhenius plot reveal E_A s of 21(2) meV for n-channel 1, 22(2) meV for n-channel 2, 30(4) meV for p-channel 3, 27(4) meV for n-channel 4, 39(6) meV for p-channel 5, 70(5) meV for n-channel 6, 75(7) meV for n-channel 7, and 250(20) meV for p-channel 4. Results are summarized in Table 3. These E_A s reveal a trend of increasing activation energy with falling room temperature μ_{eff} across the series from 0.42(2) cm² V⁻¹ s⁻¹ for 1, 0.31(3) cm² V⁻¹ s⁻¹ for 2, 0.39(4) cm² V⁻¹ s⁻¹ for 3, 0.090(3) cm² V⁻¹ s⁻¹ for n-channel 4, 0.031(2) cm² V⁻¹ s⁻¹ for 5, 0.018(1) cm² V⁻¹ s⁻¹ for 6, 0.011(1) cm² V⁻¹ s⁻¹ for 7, and finally to 0.010(2) cm² V⁻¹ s⁻¹ for p-channel 4-based FETs. Note that the behavior of 3-based FETs is

in good agreement with previous reports where pentacene exhibited $\mu_{\text{eff}} \approx 0.3$ cm² V⁻¹ s⁻¹ and $E_A = 36\text{--}40$ meV.^[15,33,34] In the present study, a slightly larger μ_{eff} and slightly lower E_A is observed which is consistent with the general trend correlating μ_{eff} with E_A .

Several models to describe charge transport mechanisms in organic materials have been proposed. These include transport in delocalized states,^[41,42] variable-range hopping,^[43] Holstein's theory of small polaron motion,^[35,44] MTR,^[23,26,28,31,37,45] and hybrid models.^[46] The data in the present study were fit to plots for delocalized charge transport ($\mu_{\text{eff}} \propto T^{0.5}$), variable-range hopping ($\mu_{\text{eff}} \propto T^{0.25}$), and MTR ($\mu_{\text{eff}} \propto 1/T$) with the least uncertainty found in their linear least-squares fits to Arrhenius plots (Fig. 1a). There is also a significant V_T displacement to higher potentials with decreasing temperature. Such a shift can be attributed to trapped charge at the semiconductor–dielectric interface that effectively screens the gate field, resulting in higher potentials needed to turn on the FET (Fig. 1b). For these reasons the results are discussed below in the context of the

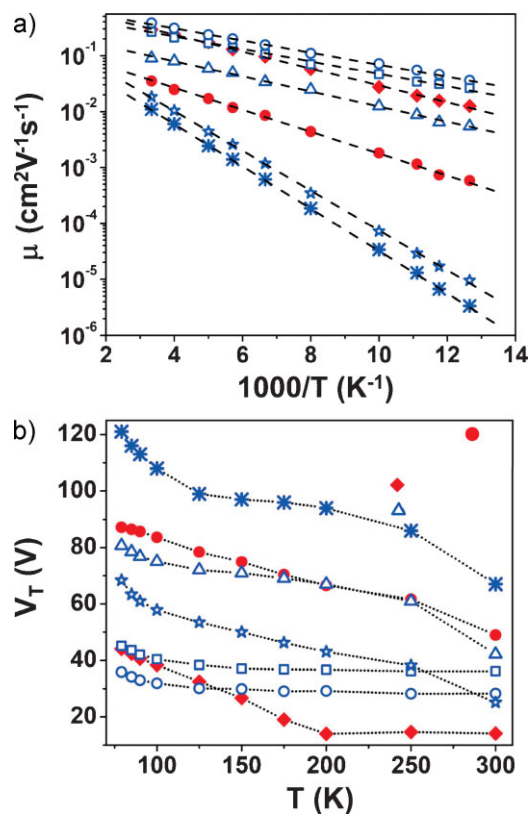


Figure 1. Plots of a) FET μ_{eff} versus inverse temperature with E_A for each of the indicated organic semiconductors and b) V_T as a function of temperature ($-V_T$ is plotted for p-channel materials). The dashed lines in (a) are least-squares fits to the Arrhenius relationship, Eq. 2, while the dotted lines in (b) are drawn as a guide to the eye. Data and fit parameters are summarized in Table 3.

MTR mechanism using the typical single-energy-level trap approximation.

These results represent the first time that a statistically significant correlation between room temperature FET μ_{eff} and E_A has been observed within a single study and over such a broad range of organic semiconductors. Moreover, the present data are also consistent with previous reports achieving satisfactory

fits to Arrhenius models, for FETs with $\mu_{\text{eff}} \geq \sim 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $E_A < \sim 50 \text{ meV}$ (entries in the bottom half of Table 1), and for $\mu_{\text{eff}} < \sim 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $E_A > \sim 50 \text{ meV}$ (entries at the top of Table 1). Significantly, the present experimental E_A s do not correlate with the conduction band energies estimated from electrochemical data (Table 2) or with majority charge carrier type (Table 2), arguing that the MTR behavior is not intrinsically tied to MO energies, but rather arises from thin-film properties such as film microstructure, crystal strain/defect sites, grain boundaries, and/or the nature/chemistry of the semiconductor–dielectric interface. This result is striking and in agreement with several other theoretical and experimental studies performed using a variety of techniques, suggesting that both n-channel, and p-channel transport experience similar trap state; distributions are not necessarily a function of specific charge transport energy levels, but rather result from more pervasive trapping/scattering phenomena in the organic semiconductors.^[19,20,42,47,48]

It is important to understand the origin and nature of the trap states that limit OFET performance for optimizing device design, fabrication, and operational stability. Indeed, these trap states appear to be equally as important for achieving high-temperature μ_{eff} as low-lying LUMO energies are for avoiding O_2 , H_2O , and surface hydroxyl trapping in n-channel FETs, and as sufficiently low highest occupied molecular orbital (HOMO) energies are to avoiding ambient doping in p-channel FETs.^[21,25,49–51] This conclusion also suggests reasons why previous reports of FET transport based on the same organic semiconductor exhibit differing variable temperature behavior, since parameters such as substrate preparation/cleaning, semiconductor purity, film growth conditions, and electrode contact can strongly influence variable-temperature transport characteristics.^[23,26,27,29,30,33,35,36]

From the data on the present materials, note that although μ_{eff} at 300 K ranges from $\sim 0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for semiconductor 1^[52] to $\sim 0.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for semiconductor 7, the values for μ_0 derived from fitting to Equation 2 reveal that in the absence of shallow trapping, these materials would all exhibit a $\mu = 0.2\text{--}0.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These results complement those in a recent study by Blom and co-workers where, using a diode device architecture, they reported that charge transport in PCBM ([6,6]-phenyl-C₆₁-butyric acid methylester) and a series of semiconducting polymers is characterized by a universal mobility (diode μ_0) of $\sim 30\text{--}40 \text{ cm}^2 \text{ V s}^{-1}$.^[53] The lower values found in the present study for FET μ_0 may reflect

Table 3. Summary of data fit parameters for FETs of semiconductors 1–7 films with standard deviations in parentheses and the first electrochemical potential (reduction for n-channel materials and oxidation for p-channel materials) of the semiconductor.

Semiconductor	Carrier type	μ_{eff} [a] [$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$]	μ_0 [b] [$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$]	E_A [b] [meV]	S [c] [V decade ⁻¹]	$N_{\text{SS}}^{\text{max}}$ [d] [cm^{-2}]	ΔN_T [e] [cm^{-2}]	$E_{\text{redox}}^{1/2}$ [f] [V]
1	n	0.42 (2)	0.83 (6)	21 (2)	6.3	6.8×10^{12}	4.7×10^{11}	-1.03
2	n	0.31 (3)	0.62 (4)	22 (2)	7.7	8.2×10^{12}	5.5×10^{11}	-0.88
3	p	0.39 (4)	0.95 (4)	30 (4)	8.9	9.5×10^{12}	1.9×10^{12}	+0.48
4	n	0.090 (3)	0.28 (1)	27 (4)	7.5	9.4×10^{12}	2.4×10^{12}	-1.06
4	p	0.010 (2)	160 (270)	248 (20)	10.4	1.1×10^{13}	-[g]	-
5	p	0.031 (2)	0.16 (2)	39 (6)	4.9	5.2×10^{12}	2.4×10^{12}	-
6	n	0.018 (1)	0.27 (1)	70 (5)	3.9	4.2×10^{12}	2.7×10^{12}	-0.45
7	n	0.011 (1)	0.19 (3)	75 (7)	14.7	1.8×10^{13}	3.4×10^{12}	-1.11

[a] Calculated using Eq. 5, [b] calculated using Eq. 2, [c] calculated using Eq. 6, [d] calculated using Eq. 3, [e] calculated using Eq. 4, [f] electrochemical half-wave potential versus SCE of the first reduction event in THF solution, [g] device output below measurable limit at $T = 79 \text{ K}$.

the lower FET versus diode electric fields and the absence in a diode device architecture of dielectric surface-related deep trapping states.^[54] The narrow range of FET μ_0 values deduced for materials 1–7 suggests that these semiconductors have similar inherent charge transporting capacities, independent of charge carrier type, and that device-level film microstructure/interface characteristics must strongly influence or even dominate the observed OFET response characteristics. This finding is consistent with other recent studies reporting that rigorous exclusion of charge traps and/or inclusion of gate dielectric interfacial layers can significantly enhance μ_{eff} in otherwise low-mobility OFETs.^[19,20,35,42,47,48,55] Furthermore, the single-crystal X-ray structures of n-channel 1 and p-channel 4 also suggest that the inherent trap-free mobilities should be comparable, since the two materials have similar packing motifs and comparable π – π stacking distances of 3.50 and 3.43 Å, respectively.^[52,56] The relatively large observed standard deviations in E_A and μ_0 for p-channel operation of the 4-based FETs suggests that device performance is strongly influenced by trapping, and the dispersion in μ_0 precludes more detailed transport mechanism analysis.

2.2. Temperature Dependence of V_T

Definitive evidence of charge trapping is observed in the temperature dependence of V_T (Fig. 1b and Fig. 2a). Semiconductors 1–7 exhibit a shift in threshold voltage (ΔV_T) ranging from 8 to

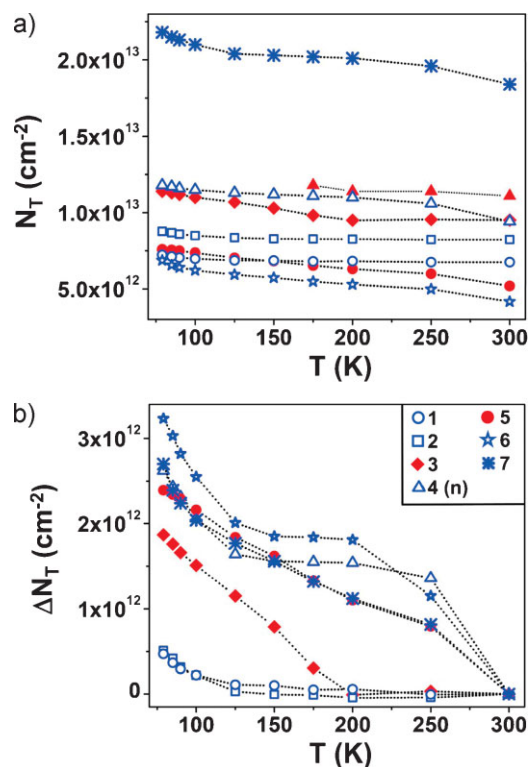


Figure 2. Plot of charge trap density (N_T) versus temperature, calculated using Eq. 6 (a), and a plot of ΔN_T versus temperature obtained from Eq. 6 (b). The dotted lines in (a) and (b) are drawn as guide to the eye.

54 V between 300 and 79 K (Fig. 2b). Such ΔV_T s have been observed previously with decreasing temperature for n- and p-channel OFETs in the range of 11–40 V (Table 1).^[26,28c,32] In those studies, however, the limited variety of semiconductors examined and/or large device-to-device variation precluded a more detailed analysis of the ΔV_T response. In the present contribution, the breadth of semiconductors studied and the small standard deviations observed in the V_T data, allow a clear correlation to be drawn between ΔV_T and the trap-limited μ_{eff} at 300 K.

The trapped charge density at room temperature (N_{SS}^{max}) can be calculated using the subthreshold swing (S) according to the established relationship^[57,58] in Equation 3, where q is the elementary charge and C_{ox} is the areal capacitance of the gate dielectric.

$$N_{SS}^{\text{max}} = \left[\frac{0.43429S}{kT/q} \right] \frac{C_{\text{ox}}}{q} \quad (3)$$

The ΔV_T can then be converted to the change in the trapped charge density ΔN_T using the previously derived relationship of Equation 4.^[17,23] These two relationships allow the trapped charge density N_T

$$\Delta N_T = q \Delta V_T C_{\text{ox}} \quad (4)$$

to be calculated at each temperature. The derived parameters (Table 3) show how the filled trap density (N_T) changes as temperature decreases and carriers cannot be thermally released from shallow charge traps. In other words, shallow traps which contribute to diminished μ_{eff} according to the MTR model, are quantified by ΔN_T . Interestingly, the plots of N_T and ΔN_T versus temperature suggest two regimes for charge trapping (Fig. 2). Similarity is seen in all curves for temperatures below 150 K, where N_T and V_T increase exponentially. This exponential behavior can be fit with the single-energy-level trapping model given in Equation 1. Fits to the data below 125 K yield the trap depths of 28–40 meV for the n-channel FETs and 17–23 meV for p-channel 3 and 5 (Fig. 3). These shallow trap energies correspond well to the shallow trap depths of ~ 20 –50 meV estimated by Frisbie and co-workers in the linear regime, applying the Meyer–Neldel relationship^[59] to PDI-based

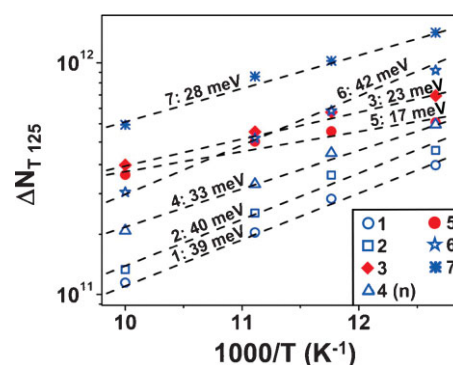


Figure 3. Plot of $\log \Delta N_T$ versus inverse temperature from 79–100 K. The dashed lines are fits to the data using Eq. 1, with the calculated trap depth indicated.

OFETs.^[23,26] Furthermore, a grain boundary trap depth for p-channel operation of α 6T-based FETs has been identified to be ~ 15 meV by Frisbie and co-workers^[13] comparable to the value obtained in this study for p-channel semiconductor 5.

A second trapping regime is observed for temperatures above ~ 200 K, where the three highest-mobility semiconductors, 1–3, exhibit negligible changes in N_T and the semiconductors with lower mobility, 4–7, show evidence of significant charge trapping with increased curvature, and $\Delta N_T \approx 2 \times 10^{12} \text{ cm}^{-2}$ at 150 K. Such divergent behavior is also evident in data of Frisbie and co-workers where PDI-based OFETs with $\mu_{\text{eff}} = 0.055 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ exhibit V_T values that increase abruptly when temperatures decrease below 300 K, while devices with $\mu_{\text{eff}} = 1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ exhibit V_T values that do not increase appreciably until ~ 170 K (estimated from the plot).^[26] Three other sets of OFET V_T versus temperature data in the literature also exhibit behavior similar to the low mobility devices in this contribution— V_T begins to shift to higher potentials as soon as the temperature falls below ~ 300 K for devices with $\mu_{\text{eff}} \leq \sim 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[28c,32] The ΔV_T behavior observed in this study is consistent with previous reports, although in the present contribution, trends within the data set can be evaluated due to the greater breadth of semiconductor properties included, control of parallel fabrication conditions, and low device-to-device variability.

Interestingly, high-mobility materials 1 and 3 do not show evidence of deep traps, while the materials with lower μ_{eff} do. This suggests that for lower μ_{eff} materials 4–7, a second regime of trapping limits FET performance. Additionally, there is no correlation between the conduction state energy and the presence of these deeper traps since, for example, the N_T curvatures for 6 and 7 are very similar, even though their LUMO energies differ by ~ 0.7 eV. Notably, the low-temperature regime for all materials can be fit to Equation 1 (Fig. 2b), where the energetic parameter observed is related to the trap depth. The N_T calculated for the deep traps of $\sim 2 \times 10^{12} \text{ cm}^{-2}$ in 4–7 is consistent with the density of grain boundary defect traps observed in previous work.^[13]

3. Conclusions

Thermally activated OFET behavior is observed in a series of organic semiconductor-based FETs that were selected for their unique and varied materials and device characteristics. Variable-temperature characterization of FETs based on this materials set reveals that there is no correlation between the conduction state energy and E_A , while there is an inverse relationship between E_A and μ_{eff} . Fits of μ_{eff} data assuming a discrete trap energy MTR model reveal low E_A parameters for high-mobility semiconductors 1–3 of 21, 22, and 30 meV, respectively, while higher E_A values of 40–70 meV are exhibited by lower mobility OFETs based on semiconductors 5–7. The first variable-temperature transport analysis of an ambipolar material (4) reveals that although n-channel operation has an $E_A = 27$ meV, the p-channel regime exhibits evidence of significantly more trapping with an $E_A = 250$ meV. Interestingly, the calculated free carrier mobility (μ_0) is found to be $0.2\text{--}0.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for all of the present materials, largely independent of μ_{eff} , and supporting a trap-limited mobility model. Finally, the effect of temperature on V_T reveals two trapping regimes with N_T exhibiting a striking

correlation with μ_{eff} . The low-temperature regime reveals trapping by shallow states with a depth ~ 40 meV and density of $\sim 10^{12} \text{ cm}^{-2}$, both consistent with the results of previous studies using different measurement techniques. This survey of the variable-temperature behavior of an organic semiconductor series reveals general trends in trapping for n-channel and p-channel operation, and the ΔV_T data suggest that at least two trapping regimes can significantly influence room temperature OFET performance.

4. Experimental

Semiconductors 1, 2, and 4–7 were synthesized and rigorously purified according to literature procedures.^[52,56,60,61] Semiconductor 3 was purchased from Aldrich and purified by multiple temperature gradient sublimations under high vacuum (10^{-7} Torr, 1 Torr = 133.32 Pa). Prime grade p-doped silicon wafers (100) having 300 nm thermally grown oxide (Montco Silicon) were used as device substrates. These were sonicated in methanol, acetone, and propanol, and were oxygen plasma cleaned before film deposition. Trimethylsilyl functionalization of the SiO_2 surface was next carried out by exposing the cleaned silicon wafers to hexamethyldisilazane (HMDS) vapor under nitrogen at room temperature for 4 days. Films of oligomers 1–6 were thermally evaporated onto substrates at their previously optimized deposition temperature (80, 90, 70, 90, and 150 °C, respectively)^[52,61,61] under high-vacuum ($< 3 \times 10^{-6}$ Torr) to a thickness of 50 nm at a QCM-monitored rate of $0.1\text{--}0.2 \text{ \AA s}^{-1}$ (QCM = quartz crystal microbalance). Films of 7 were spin-coated from 0.5% w/v CHCl_3 solutions, dried at 120 °C in vacuo for 12 h, and annealed under nitrogen at 240 °C for 2 h.^[56] The spin-coated polymer films were found to be 43 ± 7 nm thick as determined by profilometry. For FET device fabrication, top-contact gold electrodes (500 Å) were deposited by thermal evaporation at a rate of $0.1\text{--}0.3 \text{ \AA s}^{-1}$ through a shadow mask to define channels with dimensions $100 \mu\text{m}$ (L , length) \times 5.00 mm (W , width). The C_{ox} of the 300 nm SiO_2 insulator is $1 \times 10^{-8} \text{ F cm}^{-2}$, and mobility (μ_{eff}) is calculated in the saturation regime using Equation 5 within the gate voltage, V_G , range of 80–100 V for n-channel FETs, -80 to 100 V for p-channel FETs, or 110–130 V for 7 to minimize the effect of varying V_G on μ_{eff} in this study. The subthreshold swing (S) was calculated using Equation 6.

$$I_{D,\text{sat}} = \frac{W}{2L} C_{\text{ox}} \mu_{\text{eff}} (V_G - V_T)^2 \quad (5)$$

$$S = \left[\frac{d \log(I_D)}{dV_G} \right]^{-1} \quad (6)$$

The temperature of the OFET measurements was regulated using an Advanced Research Systems Helitran LT-3 open cycle cryostat controlled by a Lakeshore Cryotronics Model 331 Temperature Controller equipped with dual calibrated silicon diode temperature sensors. The cryostat was mounted in a customized high-vacuum probe station operated at pressures of $< 1 \times 10^{-6}$ Torr. Device substrates and the silicon diode used to record the temperature were mounted on a 1.0 mm thick sapphire crystal, attached to the cryostat sample stage with indium. Coaxial and/or triaxial shielding was incorporated into Signaton probes to minimize noise levels. TFT characterization was performed with a Keithley 6430 sub-femtoammeter (drain) and a Keithley 2400 (gate) source meter, operated by a locally written Labview program and GPIB communication. Variable temperature data were collected on a minimum of ten devices for each semiconductor and their figures of merit averaged at each temperature. Standard deviations were $< 15\%$ for all devices measured at a given temperature, and data collected while cooling the device from 300 to 79 K were indistinguishable from data collected while warming the device from 79 to 300 K. A ramp rate of 2.0 K min^{-1} was used when changing temperature to minimize the effect of different coefficients of thermal

expansion on the device, and post-run measurements confirmed negligible change in device performance for all OFETs.

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