Molecular Self-Assembled Monolayers and Multilayers for Organic and Unconventional Inorganic Thin-Film Transistor Applications

By Sara A. DiBenedetto, Antonio Facchetti,* Mark A. Ratner,* and Tobin J. Marks*

1. Introduction

Organic thin film transistors (OTFTs) are desired for the manufacture of low-cost electronic devices such as electronic pricetags, postage stamps, RFID tags, “smart” cards, flexible electronic paper, and backplane circuitry for active matrix displays. * While much of the attention of the organic TFT community has been focused on the search for high-mobility, ambient stable, and solution-processable small molecule and polymeric semiconductor materials, it is now clear that substantial improvements in TFT performance can also be achieved by replacing and/or modifying the gate dielectric materials: self-assembled monolayers (SAMs) and multilayers (SAMTs) of organic molecules having good insulating properties and large capacitance values, requisite properties for addressing these challenges. We first describe the formation and properties of SAMs on various surfaces (metals and oxides), followed by a discussion of fundamental factors governing charge transport through SAMs. The last section focuses on the roles that SAMs and SAMTs play in OTFTs, such as surface treatments, gate dielectrics, and finally as the semiconductor layer in ultra-thin OTFTs.

The electrical properties of SAMs composed of Cd²⁺ salts of fatty acids having different chain lengths were first characterized by Mann and Kuhn in 1971. This work led to the development of standard deposition procedures for ordered monolayers via formation of chemical bonds between the precursor molecules and the substrate/conductive electrodes. Note that although organic monolayers fabricated with the Langmuir–Blodgett technique were first reported in 1920, these films are very delicate because of the weak physisorption to the substrate. In this Review, we classify various SAM types by the material they are typically deposited on, either metals or oxides. While results for both types of substrates will be discussed, slightly more emphasis will be given to SAMs on Si/SiO₂ since this is the standard substrate/conductive electrode in the OTFT community. The article is organized as follows: after a brief overview of OTFTs in Section 1.1, we review the different methods used to deposit SAMs on metal and oxide surfaces, and introduce the fabrication of SAMTs (Section 2). A theoretical and experimental overview of SAM electronic transport is given in Section 3, and applications of SAMs as surface treatments, gate dielectrics, and active semiconducting channels in OTFTs are presented in Section 4.

1.1. Dielectrics for TFTs. Operation and Requirements

There are a number of excellent recent reviews describing the details of OTFT operation, and here we only introduce the relevant OTFT material components and basic properties. The three fundamental OTFT materials components are the contacts (source, drain, and gate), the semiconductor, and the dielectric.

As will be discussed here, self-assembled monolayers (SAMs) and multilayers (SAMTs), such as self-assembled nanodielectrics (SANDs), are gaining significant attention as gate dielectrics due to their robust insulating properties, tunable thicknesses, and efficient solution processability.
Antonio Facchetti obtained his Ph.D in Chemical Sciences (University of Milan, Italy) under Giorgio Pagani. He carried out postdoctoral research at the University of California (Berkeley, USA) with Prof. Andrew Streitwieser and then at Northwestern University with Prof. Tobin J. Marks. In 2002 he joined Northwestern University where he is currently an Associate Professor Adjunct. Dr. Facchetti’s research interests include organic semiconductors and dielectrics for thin-film transistors, molecular electronics, organic nonlinear optical materials, and organic photovoltaics.

Mark A. Ratner is Morrison Professor of Chemistry and Professor of Materials Science and Engineering at Northwestern University. He received his B.S. degree from Harvard University (1964) and his Ph.D. from Northwestern University (1969) under G. Ludwig Hofacker. He is interested in structure and function at the nanoscale, and theory of chemical processes, and tries to unite structure and function in molecular nanostructures, based on theoretical notions, exemplary calculations, and (importantly) collaborations. Interest areas are molecular electronics, self-assembly, nonlinear response, and exact and approximate theories of quantum dynamics and using nanoscience to attack the energy problems facing this world.

Tobin J. Marks is Ipatieff Professor of Chemistry and Professor of Materials Science and Engineering at Northwestern University. He received his B.S. degree from the University of Maryland (1966) and his Ph.D. degree from MIT (1971). His research interests include mechanistic organometallic chemistry and catalysis, optoelectronics, chemical vapor deposition, and molecular electronics.

Sara A. DiBenedetto is currently pursuing her Ph.D. degree under the supervision of Professors Tobin J. Marks and Mark A. Ratner at Northwestern University. She obtained her undergraduate degree in chemistry at Agnes Scott College, Decatur, Georgia (2004). Her research focuses on computational and physical chemistry for the development of hybrid organic-inorganic dielectric materials for thin film transistors.
Traditionally, OTFTs have been fabricated using a thick SiO₂ layer (usually >100 nm thick) as the gate dielectric. This material prevents gate leakage currents, acts as an effective capacitor, and allows for the accurate measurement of the electrical performance of the organic semiconducting layer. The major motivation to search for alternative gate dielectrics is to enable inexpensive fabrication (e.g., by printing near room temperature) and to significantly reduce the OTFT operating voltages. According to Equation 1 and 2, a viable approach to substantially increase the drain current, while operating at low biases, is to increase the capacitance of the dielectric,\(^{[46]}\) for a planar structure \(C = \varepsilon_0 k A / d\), where \(k\) is the dielectric constant, \(A\) the area of the electrodes, and \(d\) the dielectric thickness. However, alternative OTFT gate dielectrics should also have low gate leakage currents, and be able to sustain the maximum possible electric displacement \(D_{\text{max}} = \varepsilon_0 E_{\text{B}}\), where \(E_{\text{B}}\) is the electric breakdown field.\(^{[47–49]}\) The observable dielectric parameters, including \(E_{\text{B}}, J\) (leakage current density), and \(\varepsilon\) (dielectric permittivity) are easily measured in two terminal, planar metal-insulator-metal(semiconductor) MIM(S) devices.\(^{[1]}\)

One of the primary effects of SAMs on the response of MIM(S) and OTFT devices is the influence of a proximate molecular dipole moment on the semiconductor electron affinity or on the metal work function. The effect of a dipole layer on the surface potential can be estimated from the Helmholtz equation (Eq. 3).\(^{[50,51]}\)

\[
\Delta V = \frac{N \mu \cos \theta}{\varepsilon \varepsilon_0}
\]

Here \(N\) is the dipole density (cm\(^{-2}\)), \(\mu\) the dipole moment (debye, D), \(\theta\) the average angle the dipole makes with the surface normal, and \(\varepsilon\) is the dielectric permittivity. Numerous studies have documented how SAM dipole moment ultimately mediates the charge conduction/injection from the substrate (bottom electrode)\(^{[50,52–53]}\) and the conduction/injection through the SAM and into the semiconductor channel of the OTFT\(^{[54–56]}\). While, the main focus of this Review is on SAMs and SAMTs for use as gate dielectrics in OTFTs, it is clear from the Helmholtz relation (Eq. 3) that the interpretation of the electrical properties is complicated by the intrinsic interplay between the electrostatics of the SAM itself\(^{[50]}\) and the electrical interactions between the SAM and the underlying electrodes/semiconductors\(^{[57–61]}\) which will differ depending on the exact TFT contact geometry.\(^{[62–64]}\) Despite some of the unresolved aspects of the SAM dielectric-semiconductor interactions,\(^{[65]}\) this Review demonstrates how SAMs and SAMTs are rapidly advancing the field of plastic electronics. Therefore, we survey many aspects of SAMs that should be considered in TFT applications, starting with a description of SAMs and SAMTs having various chemical structures on metal and oxide surfaces.
2. Fabrication of SAMs and SAMTs

SAMs are ordered molecular assemblies formed by the spontaneous adsorption of an active molecular precursor onto a solid surface. Usually the precursor molecular species are dissolved in common solvents, however SAMs can be deposited by other techniques, such as vapor deposition, as well. Since there are detailed descriptions of the chemistries, structures, and characterization of various SAMs available in the literature, here we only briefly summarize the techniques and molecular structures of common SAMs and SAMTs.

2.1. SAMs on Metals

The most extensively investigated types of SAMs are alkanethiols on gold,[73–80] silver,[81–84] copper,[85–87] palladium,[88,89] and platinum[90,91] substrates. However, Au is most commonly used because it is easy to deposit as planar thin films and to pattern with conventional lithographic tools or chemical etchants. Furthermore, Au is reasonably inert to oxidation and readily binds organo thiols.[92] The most common procedure for SAM deposition is substrate immersion in a dilute solution of the target thiol at room temperature for 12–18 h (due to slow reorganization processes during film growth).[93,94] The choice of solvent, solution temperature, concentration, and immersion time are among the various factors affecting the structure of the resulting SAM.[92,95,96] Examples of thiol (R–SH) and dithiol (HS–R–SH) molecular structures (Fig. 2A) typically deposited on Au for electronic applications are alkane(di) thiols,[97–99] and those based on oligophen ylenes (OPs),[100–103] oligo(phenylenevinylene) (OPVs), and oligo(phenyleneethynylene) (OPVs).[104–109] where the labile thiacetyl (R–SAc) or disulfide (R–S–S–R) functional groups are sometimes used for substrate chemisorption instead of the R–SH group. Thiol-derived SAMs with interesting functionalities (Fig. 2B), such as terthiophenes,[110–112] azo-groups,[113–117] and tetracyanoquinodimethane,[118,119] have also been investigated. Alkane(di) thiols form densely packed and well-ordered domains of up to several hundreds of square nanometers on Au,[120] however the nature of the metal–sulfur bond and the spatial arrangement of the sulfur groups are still controversial topics. Nevertheless, alkanethiols have been termed the “benchmark” for any new technology related to molecular electronics since the tunneling electrical properties are relatively well documented/characterized.[120,121]

2.2. SAMs on Oxides

The use of organosilane precursors (RSiX₃, with X = Cl, OMe, OEt) to form monolayers requires hydroxylated substrate surfaces, including (but not limited to) the technologically relevant surfaces of SiO₂, Al₂O₃, and tin-doped indium oxide (ITO).[122–126] In the case of SiO₂ surfaces, the driving force for self-assembly is the in situ formation of siloxanes, which connect the precursor silane to the surface silanol (–Si–OH) groups via very strong Si–O–Si bonds (Fig. 3).[127] Since the substrate surfaces are amorphous, the packing and ordering of the chemisorbed organosilanes are determined by the underlying siloxane network, by interchain interactions, and by the reaction temperature.[128] Also, silanes with particularly short chain lengths and high vapor pressures [such as hexamethyldisilazane (HMDS)] can be deposited on hydroxylated surfaces from the vapor phase by simple exposure to the molecular vapor at room temperature, or by heating, or by exposure under vacuum.[68,129] Figure 3A illustrates the structures of commonly used SAM silane precursors, such as simple alkane chains octyltrichlorosilane and octadecyltrichlorosilane (OTS and ODTS, respectively), 3-mercaptopropyltrimethoxysilane (MPTMS), hexamethyldisilazane (HMDS), and various types of functionalized σ–π molecules.

Other classes of materials deposited on oxide surfaces include n-alkanoic acids (carboxylic end groups, Fig. 3B) and phosphonic acids (Fig. 3C). These classes of molecules have gained attention due to their ability to bind to a wide range of metal oxide surfaces (AgO, Al₂O₃, ITO) and to form robust SAMs of similar quality to that of thiols on Au (which may be useful for various technologies involving bottom contact electrodes other than Au).[130,131] In the case of organophosphonate SAMs, both vapor and solution deposition have been demonstrated. Using XPS it was shown that vapor-phase deposited phenylphosphonic acid (PP OA) reacts with the alumina surface to form P–O–Al bonds.[132] For a series of solution deposited phosphonate SAMs, the influence of alkyl chain length on deposition was investigated.[129] It was found that there is a distinct packing difference between short (C₁₀–C₁₄) alkyl and long (C₁₆–C₁₈) alkyl phosphate SAMs. For SAMs on TiO₂ surfaces, shorter molecules assemble into a less dense,
liquid-like structure as compared to longer chains.\textsuperscript{[129]} The difference is most likely due to strong bridging bidentate bonding with the surface for short chains, as opposed to long chains, which are stabilized via the enthalpy gain due to van der Waal interactions between the tightly packed alkyl chains.

SAMTs are becoming increasingly important as gate dielectrics in TFTs (as will be described in Section 4). There are various methods for depositing multilayer films described in the literature.\textsuperscript{[133–135]} Our group at Northwestern University has been investigating a special type of SAMTs, SANDs composed of alternating layers of $\sigma$ and $\pi$ constituent molecules. In addition, multilayers of diphosphonic acids alternating with (and held together by) Zr$^{4+}$ ions have also been demonstrated.\textsuperscript{[68,136]} See Figure 3D for examples of general molecular precursor structures used in SAMTs.

The present two-step method of fabricating SANDs (Fig. 4) involves an iterative combination of: (i) self-limiting chemisorption of siloxane building blocks, such as $\alpha,\omega$-difunctionalized hydrocarbon chains (Alk), or highly polarizable, siloxy-protected stilbazolium layers (Stb), and (ii) in situ siloxy group removal concurrent with “capping” using an octachlorotrisiloxane-derived layer (Cap).\textsuperscript{[37]} This second step deposits a robust polysiloxane layer ($\sim$0.8 nm thick), which is essential for stabilizing/planarizing the molecular layer and regenerating a reactive hydroxyl surface for subsequent monolayer deposition.\textsuperscript{[137]} The different types of multilayers are identified by the combination of different layers according to the following nomenclature: Alk + Cap (type I), Stb + Cap (type II), and Alk + Cap + Stb + Cap (type III). The microstructures and electrical properties of I–III have been characterized by specular X-ray reflectivity, standing wave X-ray reflectivity, optical absorption spectroscopy, optical second-harmonic generation measurements, atomic force microscopy (AFM), MIM(S) devices, cyclic voltammetry, and scanning electron microscopy (SEM).\textsuperscript{[1]}

2.3. SAMs on H-Passivated Si

For certain organic electronic applications (such as high capacitance gate dielectrics) it is desirable to study the direct interface between the organic SAM and Si without the influence of the native oxide layer.\textsuperscript{[70]} However, depositing SAMs directly on the Si surface requires removing the native oxide, forming a reactive surface, and changing the anchoring
generated either by hydrogen or halogen termination or by
with the H-passivated Si surface). The reactive Si surface can be
group of the molecule (since trichlorosilanes do not react cleanly
orbital (LUMO). Utilizing this wide gap, well-ordered SAMs
molecular orbital (HOMO) and the lowest occupied molecular
SAMs of aliphatic chains are expected to be dielectric in
various test-beds) can be represented by a MIM(S) structure.
One of the more extensively studied methods uses the
alcohols or organolithium/organomagnesium reactions.\[139,140\]
There are several types of surface reactions to create these types of
functionalized reconstructed surface under ultrahigh vacuum
hydrosilylation, and chemical grafting using
molecules (Section 4.3). SAMs of conjugated molecular structures have also
been extensively studied as molecular rectifiers.\[142–148\] As
congruous SAMs become more widely used in (and on) the
gate dielectric of TFTs, it is important to consider the
consequences that their smaller HOMO–LUMO gaps may have
on the conduction mechanism of the SAM.\[149\] There is abundant
literature on conduction mechanisms\[84,150–153\] and on charge
transport in SAMs;\[70,118,120,144,145,154–158\] therefore we present a
summary of some of the relevant conduction mechanisms and
the most recent results relating to various SAMs.

3. Electrical Characterization of SAMs

SAMs sandwiched between conductive electrodes (see Fig. 5
for various test-beds) can be represented by a MIM(S) structure.
SAMs of aliphatic chains are expected to be dielectric in
nature, due to the very large gap between the highest occupied
molecular orbital (HOMO) and the lowest occupied molecular
orbital (LUMO). Utilizing this wide gap, well-ordered SAMs
of alkyl chains exhibiting leakage current densities \(J \approx 10^{-8}–10^{-6} \text{ A cm}^{-2}\) have been successfully integrated in OTFTs
as surface treatments on thick oxides and as gate dielectrics
(Section 4.3). SAMs of conjugated molecular structures have also
been extensively studied as molecular rectifiers.\[142–148\] As
congruous SAMs become more widely used in (and on) the
gate dielectric of TFTs, it is important to consider the
consequences that their smaller HOMO–LUMO gaps may have
on the conduction mechanism of the SAM.\[149\] There is abundant
literature on conduction mechanisms\[84,150–153\] and on charge
transport in SAMs;\[70,118,120,144,145,154–158\] therefore we present a
summary of some of the relevant conduction mechanisms and
the most recent results relating to various SAMs.

3.1. Tunneling

Nonresonant tunneling (through bonds) is the most common
transport mechanism observed in molecular SAMs;\[159–163\]
however for \(\pi\)-conjugated molecular SAMs, resonant tunneling
(through the molecular orbitals) may also occur due to the smaller
HOMO–LUMO gap.\[164–170\] The simplest tunneling model
assumes a finite potential barrier at the metal–insulator interface
and describes the finite probability for electrons to travel a short
distance into the SAM (or insulator) despite the lack of available
energy levels. This processes is given by the Simmons relation
(Eq. 4), which is expressed here in the simplest form for a
rectangular barrier to demonstrate the exponential dependence of
the current density \(J_{\text{DT}}\) on the thickness (\(d\)) and barrier
height (\(\phi\)).\[70,144\]

\[
J_{\text{DT}} = \frac{q^2 V}{h^2 d} \left(2m\phi\right)^{1/2} \exp\left(-\frac{4\pi d}{h} (2m\phi)^{1/2}\right)
\]

where \(q=\text{electron charge, } V=\text{applied voltage, } h=\text{Planck's constant, and } m=\text{electron mass. At low voltages Equation 4 can be simplified to } J_{\text{DT}} \propto (1/d) \exp(-\beta d)\), where the tunneling
decay parameter, \(\beta\) (Eq. 5).

\[
\beta = \frac{4\pi (2m\phi)}{h} \alpha
\]

is accepted to be \(0.6–1 \text{ Å}^{-1}\) for saturated alkanes, and \(0.2–0.6 \text{ Å}^{-1}\)
for \(\pi\)-conjugated molecules, and smaller \(\beta\) indicates more
efficient tunneling.\[145\] Here \(\alpha\) is a unitless parameter describing
asymmetry of the potential profile (\(\alpha=1\) for a rectangular
barrier). For very large applied voltages \((V > \phi)\) the barrier
changes to a triangular shape, and the tunneling current is given by
the Fowler–Nordheim equation (Eq. 6).\[70,172–175\]

\[
J_{\text{FN}} = \frac{q^2 E^2}{8\pi h \phi_{\text{FN}}} \exp\left(-\frac{4\sqrt{2m^*}}{3q\phi E} (\phi_{\text{FN}})^{3/2}\right)
\]

Here \(\phi_{\text{FN}}\) is the tunneling barrier height, \(E\) the electric field
\((V/d)\), and \(m^*\) is the effective electron mass. Fowler–Nordheim
emission has the strongest dependence on the applied voltage,
but (like Eq. 4) is essentially independent of the temperature
(since it is a pure electronic tunneling).
Conduction in SAMs also depends on the nature of the chemical linker that binds the molecule to the bottom metal electrode.\cite{176,178} For example, the conductance differences within a series of 1,4-butylene alkanes terminated with dimethyl phosphine, methyl sulfide, or amine (Fig. 6C) was compared.\cite{179} The authors assumed nonresonant tunneling as the dominant conduction mechanism, and found that phosphine termination provides the lowest contact resistance (highest conductance) of the series. Similarly, a correlation between molecular structure and electrical resistance (R) in the nonresonant tunneling regime was demonstrated in another study by a systematic comparison of alkyl versus conjugated and mono- versus di-thiol substituted bridging molecules (Fig. 6D).\cite{180} Based on a multi-barrier tunneling model,\cite{181} for a given chain length R, the resistance of the monothiol junction was roughly 2x greater than the di-thiol junction, most likely due to the properties of the chemisorbed versus physisorbed nature of the top contact. Interestingly, the contact resistance of the alkane dithiols and their conjugated analogs were found\cite{180} to be similar and independent of the differing HOMO–LUMO gaps of the different molecular structures.

The conduction mechanism of SAMs on oxide surfaces is far less developed than for SAMs on Au. For example, in 1996 Vuillaume et al. reported a suppression of tunneling in metal/alkylsilane/SiO$_2$/Si structures, resulting in low conductivities (which is advantageous for TFT gate dielectric applications as will be discussed in Section 4). The conduction was shown to be independent of monolayer thickness (Fig. 7A), indicating that tunneling is not the dominant conduction mechanism, however no alternative mechanism was suggested.\cite{182} In 1999, Waldeck and co-workers performed photocurrent measurements on Si/SiO$_2$ coated with different alkyllsilanes and observed a much weaker dependence of the conduction on monolayer thickness than expected (Fig. 7B), and the authors suggested hopping through traps in the film (see below) as a possible mechanism to explain the weak distance dependence.\cite{183} In 2002, Cahen and co-workers measured the conductance through alkanes in Hg/alkylsilane/SiO$_2$/Si MIS devices.\cite{185} The results are striking since at first glance it would appear that there is a clear dependence of the current density on the chain length (Fig. 7C). However, the authors explained that the curves are essentially identical within the experimental uncertainty. The results are then in agreement with the results from the earlier studies, where the conduction in alkyllsilanes on native SiO$_2$ does not depend on chain length. Furthermore, the J values of 10$^{-6}$ A cm$^{-2}$ at 1 V are lower than the theoretical model for tunneling, even with an added tunneling barrier (where the added barrier was included to account for the possibility that not all of the silane chains are bonded to the SiO$_2$).

As an example, conduction through SAMs derived from α-substituted aromatic or heteroaromatic alkanethiols (Fig. 6A) was investigated in Au–SAM–Au junctions, where the top Au electrode was deposited by cathodic deposition directly on top of the monolayer.\cite{176,179} High breakdown field strengths ($E_b$)$>$50 MV cm$^{-1}$ were measured, and it was concluded that the terminal aromatic rings have strong π–π interactions which densify the surface, hindering the penetration of metal. Furthermore, the authors modified the typical square-well tunneling potential to fit the J–V data within the direct tunneling model, but did not investigate the J(V, T) dependence. In a recent study, “edge” molecular junctions were used to investigate the electrical properties of conjugated 4,4’-biphenyldithiol (BPDT) SAMs compared to an aliphatic C$_9$ dithiol alkyl SAMs (Fig. 6B).\cite{177} The top electrode (either Ag or Au) was vapor-deposited at reduced temperatures and at a 60° angle to create the edge structure. Conduction through the conjugated BPDT SAM was determined to be via tunneling, despite the larger currents and smaller HOMO–LUMO gap than in the C$_9$ SAM.
Again, the authors suggest hopping as the transport mechanism since the barrier heights are similar to those for hopping in other bilayer structures.\[121,184\]

3.2. Thermally Activated Processes

Hopping refers to Ohmic transport, which is typically dominant at low fields and moderate temperatures. For simple hopping, \( J \) follows a classical Arrhenius relation (Eq. 7),\[152,185\]

\[
\sigma = \sigma_0 \exp\left(\frac{-E_a}{kT}\right)
\]

where \( \sigma \) is the conductivity, \( \sigma = J/E \) (\( E = V/d \)), and \( E_a \) is the activation energy. McCreery\[144\] associated hopping with nuclear motion (or molecular reorganization), and Bässler and co-workers\[186–188\] proposed that hopping occurs among large defects or impurities. Whatever the origin of the hopping, it is observed much less frequently in SAMs than is tunneling because the typical lengths of the molecules investigated are seldom greater than \( \sim 2 \) nm.\[162,189,190\]

Extensive theoretical work has been reported concerning the tunneling/hopping transition,\[154,191–197\] and earlier data on some organics\[198–201\] and DNA\[202,203\] have clearly revealed a length dependent transition between tunneling and hopping conduction. Recently, the transition was demonstrated in Au-molecule-Au junctions, where the electrical resistance of oligophenyleneimine (OPI) molecules of various lengths were measured with a conductive AFM tip (Fig. 8).\[204\] Hopping transport was found in OPI molecules longer than 4 nm, while molecules \(< 4 \) nm in length exhibited nonresonant tunneling. Furthermore, the authors intentionally disrupted the molecular conjugation with cyclohexyl groups and found that conduction in molecules with hopping transport (>4 nm length) was affected far more than molecules with tunneling transport (<4 nm in length).

In one of the earliest conduction studies, thermally activated transport through SAMs of thioacetylbiphenyl\[205\] (molecular length \( \sim 1.2 \) nm) in Au/SAM/Au nanopore devices (Fig. 5E) was attributed to hopping. Using a physisorbed aryl-Ti top contact, the SAM/Au barrier height was estimated to be 0.22 eV according to the thermal emission (Schottky emission, see below) model. For the direction of transport through the Au-thiol bond (negative applied voltages), the authors proposed hopping transport through the SAM with a barrier of 0.19 eV (Fig. 9A). However, these authors pointed out that the nature of the hopping barrier (defects in the SAM, hopping along the wire, or between molecules) is unclear. In 1999, this work was extended to...

elucidate the nature of hopping in conjugated SAMs\cite{206} by investigating phenylene disocyanide in similar nanopore devices (Fig. 9B). It was observed that the dominant conduction mechanism depends on the defect level introduced during the fabrication process. For very large defect densities (typically in devices with evaporated metal contacts), only hopping was observed with a barrier of $\sim 0.3$ eV. However both hopping and thermionic emission (see below) were observed when the defect level was reduced (with corresponding barrier heights similar to the previous study of thioacetylbiphenyl SAMs).

The energy distribution of electrons in metals is given by the Fermi–Dirac distribution function. This implies that at elevated temperatures (and at larger applied biases than for hopping) a larger fraction of the electrons will have sufficient energy to surmount the energetic barrier presented by the SAM. Thermionic (Schottky) emission (Eq. 8) assumes that an electron from the contact can be injected into the dielectric once it has acquired sufficient thermal energy to cross the potential barrier presented by the SAM.

Thermionic (Schottky) emission (Eq. 8) assumes that an electron

\begin{equation}
J_S = A^*T^2 \exp \left(-q\left(\phi_b - \sqrt{qE/4\pi\varepsilon\varepsilon_0}\right)/kT\right)
\end{equation}

where $\phi_b$ is the barrier height, $k$ is the Boltzmann constant, $q$ is the electron charge, and $E$ is the electric field.

\begin{equation}
J_{PF} \propto E \exp \left(-q\left(\phi_{PF} - \sqrt{qE/4\pi\varepsilon\varepsilon_0}\right)/kT\right)
\end{equation}

Since both mechanisms result from Coulombic lowering of the potential barrier under an applied electric field, the two processes have similar $J(V,T)$ dependencies. The square root term for Poole–Frenkel emission is greater than Schottky emission by a factor of 2, and often the exponent of Eq. 8 and 9 are simplified by introducing a $\beta$ parameter $[\beta_S = (q\sqrt{4\pi\varepsilon\varepsilon_0})^{1/2}$ and $\beta_{PF} = (q\sqrt{4\pi\varepsilon\varepsilon_0})^{1/2}$. Here, $\beta_S$ is the modified Richardson’s constant ($A^* = 120$ $A \text{ cm}^{-2} \text{ K}^{-2}$) $E$ is the electric field, $\phi_b$ and $\phi_{PF}$ are the Schottky and Poole–Frenkel barrier heights, $\varepsilon$ is the dielectric permittivity, $\varepsilon_0$ is the permittivity of vacuum, and $k$ the Boltzmann constant.

As an example, thermally activated defect conduction was also observed in cross-linkable organo-siloxane hybrid dielectrics, synthesized by a sol–gel process\cite{209}. The leakage current characteristics were described by a Poole–Frenkel emission mechanism, related to traps in the bulk of the film. In this case, the films are much thicker (260 nm) and the material is not self-assembled. However, since the capacitor layer (Fig. 4) of SANDs is also a crosslinked siloxane, it is worthwhile to mention briefly the electronic properties of these alkoxysilane hybrid dielectrics. From ATR-FTIR spectra (Fig. 10A), the authors observed a reduction of the silanol $v(Si–OH)$ peak intensity and enhancement of the transition corresponding to the siloxane bond $v(Si–O–Si)$ with increasing film annealing temperatures (150, 170, and 190 $^\circ$C). Furthermore, the leakage current density $\left(10^6–10^5 \text{ A cm}^{-2} \text{ at } 2 \text{ V}\right)$ is lower for the films annealed at 190 $^\circ$C versus those annealed at 150 $^\circ$C. The authors fit the $J–V$ data according to the Poole–Frenkel mechanism and found that the $\beta$ parameter value extracted from the slope of the fits matched the $\beta$ parameter estimated from $\beta_{PF} = (q\sqrt{4\pi\varepsilon\varepsilon_0})^{1/2}$. Since Poole–Frenkel emission is related to thermal excitation of trapped electrons into the insulator conduction band, and since it has been reported that electrons can be deeply trapped in hydrated thermal silicon oxides (forming SiO$^-$)\cite{210} the authors proposed that the silanol groups act as trap sites (Fig. 10B) in the electronic properties of these alkoxysilane hybrid dielectrics.

Recently, inkjet printing of these materials for gate dielectrics in TFTs was demonstrated\cite{211} which is important for the low cost development of low leakage current gate dielectrics. Deposition of a high capacitance self-assembled SAM has yet to be demonstrated, although very recently inkjet printed source/drain electrodes were utilized in top contact TFTs with a SAM-based gate dielectric\cite{212} and organic single-crystal TFT arrays were demonstrated by relief printing of thick (~13 nm) OTS films\cite{213}.
current densities do not follow the typical dependence for tunneling (Fig. 10B). Also, hysteresis and negative differential resistance were observed from the SAMT devices, but not from the monolayer devices. The authors suggested that the transport in APTMS SAMTs is hopping. The Northwestern group has also investigated annealing conditions and conduction mechanisms in SAMTs (Fig. 4). For example, it was found that SAND leakage current densities do not change significantly with increasing annealing temperatures (see Section 4.3.1.1 for results with multiple layers of III), suggesting similar transport in SAND Cap layers to the crosslinked alkoxysilane network described above. To further probe the conduction of SANDs, the J(V,T) transport characteristics of for II and III were studied over the temperature range of −65–100 °C. We find (in unpublished data) slightly different conduction in II versus III as might be expected from the different interfaces (γ vs. σ, respectively) and thicknesses (3.2 and ~6.0 nm, respectively). Analysis of the J(V,T) characteristics according to tunneling and injection models will be reported shortly.

4. TFT Device Applications

In the previous sections we introduced the importance of molecular orbital alignment, since SAMs with different HOMO–LUMO gaps and/or dipoles can shift the metal work function/semiconductor electron affinity and change the barrier to conduction. In this section, we highlight some experimental results where SAMs are used as surface treatments in devices to modify electron injection.

4.1. Metal Surfaces/Bottom Contact TFTs

Practical device technologies will most likely depend on prefabricating of the metal electrodes for bottom contact TFTs and integrated circuits. In this configuration, the major challenge is increased contact resistance arising from several effects such as interfacial charge migration, surface dipoles, the insulating nature of semiconductor side chains, or physical delamination/dewetting. Therefore, a major potential enhancement of SAMs in bottom contact TFTs is the possibility of reducing contact resistances by enhancing the semiconductor adhesion and growth orientation relative to the metal source/drain electrodes. For the commonly used organic semiconductor, pentacene (P5, Fig. 1), surface modification is essential to enhancing bottom contact TFT performance since optimal wetting of the substrate is essential for favorable large-grained first layer P5 growth.

As an example, surface treatment of Au bottom contact source/drain electrodes with simple alkanethiols (such as 1-hexadecanethiol) have been shown to modify the surface energy such that large P5 crystal grains form over large areas—both on top of and between the source/drain electrodes. These TFTs exhibit a significant increase in P5 mobility (Fig. 11A) from 0.16 cm² V⁻¹ s⁻¹ (without a SAM) to 0.48 cm² V⁻¹ s⁻¹ (with a P5 growth).
SAM). However, alkanethiols in general have a large energy gap between the HOMO and the LUMO, typically $E_G \sim 6 \text{ eV}$, and hence are good insulators. Due to the insulating behavior, reduced charge carrier injection is expected, which makes alkanethiols not suitable as contact “primers” for OTFTs. In contrast, aromatic SAMs have smaller MO gaps and hence are of interest for functionalization of bottom contact electrodes in TFTs.

To this end, several groups focused on comparing the effects of aliphatic versus aromatic SAMs on the device performance of bottom contact TFTs (see Fig. 2, e.g., of molecular structures). The two major advantages of using aromatic SAMs instead of aliphatic SAMs are increased $I_{on}/I_{off}$ ratios due to favorable electron injection,[226–228] and increased wettability of the SAM surface by the semiconductor due to SAM-semiconductor attractive interactions (Fig. 11B), both of which lower the contact resistance and improve TFT performance.[229,230] In this example, generally improved bottom contact TFT device characteristics were achieved with an aromatic anthracene-2-thiol SAM (on/off ratio of $10^6$ and strongly reduced trap density as indicated by the low subthreshold swing of 0.55 V decade$^{-1}$). AFM and SEM images revealed significant dewetting of 5 films on untreated Au electrodes, but no dewetting on both aliphatic and aromatic thiol SAM treated Au electrodes (Fig. 11B). The authors concluded that the contact resistance observed in TFTs without SAMs is related to morphological irregularities. However, since the 5 film morphology is similar on both aromatic and aliphatic SAMs, the contact resistance in TFTs with aliphatic SAMs must arise from poor electron injection.[225]

In an effort to correlate molecular structure with TFT performance, Katz et al. screened a series of thiols and other commercially available sulfur reagents with a variety of terminal functional groups as surface treatments for TFTs using a fluorinated naphthalenediimide derivative as the semiconductor layer.[221] Several of the thiol treatments provided a beneficial effect compared to devices with untreated electrodes. The highest TFT $I_{on}$ currents were obtained with 2-chlorobenzyl mercaptan, and the current enhancements were attributed to increased wetting or sticking of the semiconductor to the thiol-treated gold surface versus bare gold, due to either favorable aryl–aryl interactions or to COOH-carbonyl hydrogen bonding between the SAMs and the semiconductor (rather than due to different dipole moment strengths).

In a different approach for SAM-Au treatment, lower contact resistance was demonstrated by directly coupling a molecular monolayer similar in structure to that of 5 (the thioketone in Fig. 12A) to the source/drain electrode surface prior to 5 deposition.[229] In this configuration, the semiconductor SAM “surface treatment” acts as a template for enhanced 5 growth, and significant enhancement of TFT response characteristics over the untreated and small molecule-thiol treated bottom contact TFTs was observed. Recently, injection barrier effects of various SAMs [thiophenol (TP), 4-fluorothiophenol (4-FTP), or pentafluorothiophenol (PFTP)] on bottom contact TFT performance were investigated using TIPS-pentacene as the semiconductor (see Fig. 12B for molecular structures, TFT electrical characteristics, and proposed energy level diagram).[227] No TIPS-pentacene film morphology change was observed for films deposited on both the SAM-treated and bare Ag electrodes. However, a significant work function shift was measured (from 4.14 to 5.35 eV) by electrode treatment with the SAMs, and as a result enhanced TFT performance with SAM treated electrodes was attributed to better alignment of the modified metal work function with the semiconductor HOMO level. In untreated devices the Ag work function (4.7 eV) and semiconductor HOMO energy level (5.3 eV) mismatch creates a hole injection barrier of 0.6 eV. However, Ag surface modification with 4-FTP or PFTP dipolar SAMs modifies the work function to 5.21 and 5.35 eV, respectively, significantly reducing the injection barrier and creating an ohmic contact with reduced contact resistance.

### 4.2. Oxide Surfaces/Top Contact TFTs

One overall goal in the organic electronics field has been to enhance OTFT performance to reach metrics comparable to
amorphous hydrogenated silicon (a-Si:H), the current material used in fabricating thin film transistors (TFTs) for LC displays, which exhibits an electron carrier mobility of $\sim 1.0 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ and an $I_{\text{on}}/I_{\text{off}}$ ratio $>10^4$. PS is one of the most promising organic semiconductors for use as the active material in OTFTs because of its relatively high mobility and large TFT $I_{\text{on}}/I_{\text{off}}$ ratios, which are comparable to or surpass those of amorphous silicon.$^{233}$ Thus, many studies have employed SAM-modified SiO$_2$ as the gate dielectric and PS as the semiconductor (Table 1) to elucidate fundamental correlations between dielectric–semiconductor interfacial effects and TFT performance (see ref. $^{242}$ for a recent review).$^{233}$ Typically it is observed that SAMs (as gate dielectric surface treatments) in OTFTs achieve one or more of the following: reduce the device subthreshold slope, increase the semiconductor mobility, increase the $I_{\text{on}}/I_{\text{off}}$ ratio, alter the polarity of the majority charge carrier type, modulate the carrier density in the channel, and shift the threshold voltage (compared to control devices with bare gate dielectric oxides).$^{65,232}$ Explanations for the overall performance enhancements are usually described in the context of the semiconductor film growth morphology$^{235,231}$ (crystallinity and grain size), and/or the dielectric–semiconductor interfacial properties$^{233}$ (such as surface energy, trap sites, molecular chemical functionality, and the structure of the SAM itself).

The first indications that the dielectric–semiconductor interface has a large influence on the overall OTFT performance were the observations of: (i) different measured mobility values for the same organic semiconductor, and (ii) different film growth characteristics on different types of gate dielectrics. For example, in 1997 Gundlach and co-workers deposited PS on LiF and SiO$_2$ surfaces, and reported distinct differences in the AFM images of PS films of varying thicknesses.$^{234}$ In 1992 Horowitz et al. measured different mobility values for films of the 6T (sixithiophene, Fig. 1) semiconductor on different oxide and polymer gate dielectrics.$^{235}$ and in 2005 Muccini and co-workers studied the supermolecular organization of thin films of 6T on SiO$_2$ for a correlation between intermolecular interactions and transport properties as compared to 6T single crystals, which have mobilities up to $20 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$.$^{236}$ In a later study Horowitz et al. used AFM images of very thin (1 nm) to thicker (7.5 nm) PS films deposited on top of 1-phosphonooctane SAMs (using Al/Al$_2$O$_3$ substrates) to confirm that the PS growth mode is different when the growth is near the dielectric surface compared to growth in the bulk (Fig. 13A)$^{237}$ In this case, the average PS mobility was $2 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ (largest value $\sim 3 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ on the 1-phosphonohexadecane SAM), which was a significant improvement over the bare alumina control TFT of 1.1 $\, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$. The authors claimed near single-crystal quality PS growth during the early stages of deposition, which explains the large observed mobilities of the TFT devices since the first few monolayers of the semiconductor film are the active charge transport region.$^{237}$

In 2006, Mottaghi and Horowitz observed similar differences in PS growth modes on bare versus eicosanoic acid (CH$_3$(CH$_2$)$_{18}$COOH) SAM modified Al/Al$_2$O$_3$ gate dielectrics.$^{238}$ The PS films were modeled as multi-layer dielectrics, and it was found that the bulk PS mobility increases linearly with the gate voltage up to about 5 V on the SAM-coated Al/Al$_2$O$_3$ and 10 V on bare Al/Al$_2$O$_3$, then saturates at large values of $\sim 5 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ and $\sim 3 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$, respectively (Fig. 13B), confirming that the semiconductor mobility and growth mode are sensitive to the dielectric–semiconductor interface.

Since, these pioneering studies, many research efforts have been devoted to the investigation of the dielectric–semiconductor interface, and major improvements in the OTFT electrical characteristics have been documented.$^{239–248}$ For example, Forrest and co-workers observed major TFT mobility and $I_{\text{on}}/I_{\text{off}}$ enhancement when using OTS-treated gate dielectrics in PS TFTs, from 0.06 $\, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ and $I_{\text{on}}/I_{\text{off}} \sim 10^3$ on bare SiO$_2$, to as large as 1.2 $\, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ and $I_{\text{on}}/I_{\text{off}} \sim 10^8$ on OTS treated SiO$_2$.$^{249}$ Schwartz and co-workers found dramatic improvements ($I_{\text{on}}/I_{\text{off}}$ ratios of $10^8$ and subthreshold slopes of 0.2 V decade$^{-1}$) over other devices using octadecylsilane and other phosphonates.$^{250}$ In this study, a new (anthracene)phosphonate SAM was reported (Fig. 14C), and compared to the other

Table 1. Comparison of pentacene OTFT performance on various oxide gate dielectric surface treatment SAMs ($\mu$ [cm$^2$ V$^{-1}$ s$^{-1}$], current on/off ratio $I_{\text{on}}/I_{\text{off}}$, threshold voltage $V_T$ [V], and subthreshold slope $SS$ [V decade$^{-1}$]).

<table>
<thead>
<tr>
<th>Reference</th>
<th>SAM + Oxide</th>
<th>$\mu$ [cm$^2$ V$^{-1}$ s$^{-1}$]</th>
<th>$V_T$ (SS)</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>[233]</td>
<td>OTS + SiO$_2$</td>
<td>0.4 (10$^7$)</td>
<td>(1.6)</td>
<td>1997</td>
</tr>
<tr>
<td>[244]</td>
<td>OTS + SiO$_2$</td>
<td>0.6 (10$^7$)</td>
<td>(0.6)</td>
<td>2002</td>
</tr>
<tr>
<td>[236]</td>
<td>1-Phosphonooctane + Al$_2$O$_3$</td>
<td>2.1 (1.7 × 10$^8$)</td>
<td>−2.1(2.5)</td>
<td>2003</td>
</tr>
<tr>
<td>[237]</td>
<td>Alkylsilane + SiO$_2$</td>
<td>0.13 (10$^7$)</td>
<td>5.0</td>
<td>2004</td>
</tr>
<tr>
<td>[241]</td>
<td>Perfluoralkylsilane + SiO$_2$</td>
<td>0.20 (10$^7$)</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>[231]</td>
<td>Aminooalkylsilane + SiO$_2$</td>
<td>2.4 × 10$^7$</td>
<td>−11</td>
<td>2005</td>
</tr>
<tr>
<td>[242]</td>
<td>HMDS + SiO$_2$</td>
<td>0.2 (10$^7$)</td>
<td>−8.0</td>
<td>2005</td>
</tr>
<tr>
<td>[242]</td>
<td>poly(mide-Piloxane) + SiO$_2$</td>
<td>0.11(10$^7$)</td>
<td>−8(3.1)</td>
<td>2005</td>
</tr>
<tr>
<td>[237]</td>
<td>Eicosanoic acid + Al$_2$O$_3$</td>
<td>0.25(10$^7$)</td>
<td>−7.2(2.3)</td>
<td>2006</td>
</tr>
<tr>
<td>[239]</td>
<td>HMDS + SiO$_2$</td>
<td>0.5 (10$^7$)</td>
<td>1.1(2.9)</td>
<td>2006</td>
</tr>
<tr>
<td>[234]</td>
<td>HMDS + Al$_2$O$_3$</td>
<td>0.01(10$^7$)</td>
<td>1.2(4.1)</td>
<td>2006</td>
</tr>
<tr>
<td>[245]</td>
<td>(9-Anthracene)phosphonate + SiO$_2$</td>
<td>(10$^7$)</td>
<td>−4.5(0.2)</td>
<td>2007</td>
</tr>
<tr>
<td>[254]</td>
<td>β-Phenethyltrichlorosilane</td>
<td>1.5(10$^7$)</td>
<td>−18</td>
<td>2007</td>
</tr>
<tr>
<td>[258]</td>
<td>ODTs disordered + SiO$_2$</td>
<td>0.3(10$^7$)</td>
<td></td>
<td>2008</td>
</tr>
<tr>
<td>[258]</td>
<td>ODTs ordered + SiO$_2$</td>
<td>0.6(10$^7$)</td>
<td></td>
<td>2008</td>
</tr>
</tbody>
</table>
organophosphonate SAMs tested. The anthracene-based SAM exhibited the best TFT performance. The authors ascribed the improvements to structural similarities between P5 and the SAM substituent, which resembles a continuous anthracene film, thus providing nucleation sites for favorable growth of P5 islands. Similarly, Mottaghi and Horowitz[238] explained OTFT performance enhancements related to P5 grain size using the multiple trapping and release model. If the initial increase in bulk P5 mobility with gate voltage can be explained by filling of traps located in grain boundaries, then the smaller, more regular P5 grains observed on SAM treated Al/Al2O3 should (and do) perform better than the larger, more irregular grains observed on bare Al/Al2O3.

Correlations between P5 film grain size/crystallinity and TFT mobility have been studied in great detail[219,249,251–255] however exact trends remain unclear[1,45,256] and the behavior is entangled with other effects (surface energy,[36] surface roughness,[257] and molecular structure[258]). For example, high aqueous contact angles (80°–115°), or more hydrophobic substrate surfaces, typically result in the largest OTFT performance increase. However, it is not always simple to isolate the unambiguous origin of the improved performance. Cho and co-workers, deposited P5 on ordered (alkyl chains aligned and packed) and disordered (loosely oriented alkyl chains) OTDS SAMs (Fig. 15A), and a barrage of structural techniques were used to analyze the structural and morphological characteristics of both the OTDS and the P5 films[259]. While the surface energy and surface roughness of the two OTDS SAMs were measured to be the same, the OTFT performance observed in the more ordered SAM. X-ray diffraction spectra (Fig. 15B) of the P5 films revealed more crystalline P5 films when deposited on ordered versus disordered SAMs. Furthermore, a larger diffraction peak intensity ratio of the thin-film phase to the bulk phase was observed for the more ordered SAMs, indicating that P5 deposited on the more ordered OTDS monolayer is more sensitive to interactions with the surface since the thin-film phase is the surface-induced (strained) phase[259]. In another example, the grain size of P5 films was reported to be unchanged when deposited on HMDS-treated SiO2 and bare SiO2; nevertheless, differences in the OTFT performance characteristics were again observed.[252] In this case, it was proposed that the suppressed off-currents observed for HMDS-treated devices were due to a reduction in the density of interfacial trapping states.[260,261]

Strong evidence for this interfacial trapping effect was presented by Friend and co-workers in 2005.[210] In this study, the authors used multiple-reflection attenuated-total-reflection FTIR spectrometry (ATR-FTIR) to track the changes of the Si–OH stretching and bending combination band near 3 800–4 700 cm−1 with time and applied voltage. Based on the long times associated with peak intensity changes and wavelength shifts compared to the time for loss of TFT activity, the authors proposed that the spectral shifts were due to the generation of SiO− induced by deeply trapped electrons, indicating electrochemical trapping of electrons by SiOH surface groups. The interfacial trapping effect was observed in OTFTs using the
polymer F8BT [poly(9,9'-dioctylfluorene-co-benzothiadiazole)] as the semiconductor and alkyl-SAMs of various lengths: hexamethyldisilazane (C1), decyltrichlorosilane (C10) and ODTS (C18) as Si/SiO2 gate dielectric surface treatments. Initially, enhancement of the n-channel TFT performance was observed with increasing alkyl-SAM chain length (Fig. 16) and surface –OH passivation. However, TFT currents eventually degraded over time, and since siloxane-terminated SAMs cannot completely eliminate surface SiOH groups, the degradation was attributed to those trap sites at or near the SiO2 interface. This study not only demonstrates the importance of the dielectric–semiconductor interface on TFT performance, but also demonstrates that SAM modification benefits not only p-type (P5) TFT characteristics but also a wide range of n-type semiconductor materials.[7,8,244,262]

Lastly, the chemical composition of the semiconductor–dielectric interface can directly tune the semiconductor characteristics in a different way. In addition to charge carrier inversion (from p- to n-), it has been shown that the chemical structure of the SAM molecules can modify the carrier density in the semiconductor channel and induce appreciable threshold voltage (V_T) shifts. For example, P5 and C60 I_TD currents were observed to depend strongly on the SAM molecular structure, where the currents at V_G = 0 V were enhanced by six orders of magnitude in devices with SAMs composed of perfluoroalkylsilane molecules compared to devices fabricated with aminoalkylsilane SAMs (Fig. 17A).[258] The V_T values were shifted for the amino- and fluoro-functionalized SAMs, however the V_T values for the unsubstituted alkylsilane SAM and untreated devices were essentially the same, suggesting that the additional carriers in the semiconductor channel are generated by the built-in potentials created by the different SAM dipole moments.

In 2007, Katz and co-workers capitalized on this effect to fabricate complimentary circuits.[263] Using a nonpolar silane, PTS (phenyltrimethoxysilane), and a series of fluorinated dipolar silanes trichloro(3,3,3-trifluoropropyl)silane (FPTS), trichloro1H,1H,2H,2H-perfluorooctyl)silane (FOTS), and trichloro(1H,1H,2H,2H-perfluorodecyl)silane (FDTS), they demonstrated control over the “doping” level of the p-type semiconductor 5,5'-bis(4-hexylphenyl)-2,2'-bithiophene (6PTTP6) and fabricated unipolar inverters (see Fig. 17B for structures). Where the enhancement-mode TFT uses the p-type semiconductor 6PTTP6 with the nonpolar PTS SAM (since this SAM induces a slight negative V_T shift the device is “normally-off”), and the depletion-mode TFT uses 6PTTP6 with the polar fluorosilanes (since these SAMs exhibit a positive V_T shift they are “normally on”). The conclusion is that SAMs can induce a controllable V_T shift and modulate the current in logic circuits without the need for external electric field poling. This represents one of the best examples of how fundamental insights concerning the SAM–semiconductor interaction enable technological advances.

An alternative surface functionalization approach has recently been demonstrated by Podzorov and co-workers,[264] where organosilane SAMs deposited on the surface of single crystal rubrene (Fig. 1) induce a pronounced increase of the surface conductivity $\sigma = 10^{-5}$ S square$^{-1}$, compared to $10^{-8}$–$10^{-7}$ S square$^{-1}$ typically observed in OTFTs.[258] In this work, top gate OTFTs were fabricated on the SAM-functionalized single crystals.
using parylene as the gate insulator and observed $\mu$'s of 1–2 cm$^2$ V$^{-1}$ s$^{-1}$. Although these mobilities are lower than the highest reported,[265] and the details about SAM growth and surface binding remain unclear, the enhanced conductivity observed with SAM functionalization is promising for top gate OTFT applications utilizing the SAM as the gate insulator (instead of as a surface treatment) between the single crystal channel beneath and the deposited gate electrode on top.

4.9. SAMs and SAMTs As Gate Insulators

The notion of high capacitance SAMs and their use as the gate dielectric in OTFTs (Table 2) was pioneered by Vuillaume et al. in 1996 where it was established that SAMs of n-ODTS grafted on Si native oxide were good insulators ($C_24 > 10^{10}$ Ac m$^{-1}$ at 5.8 MV cm$^{-1}$ and breakdown at 9–12 MV cm$^{-1}$) despite a thicknesses of only 2.8 nm.[38] The authors demonstrated that the interface state density ($D$) of the OTS SAMs can be reduced by 1 order of magnitude ($2 > 10^{11}$ cm$^{-2}$ eV$^{-1}$) by annealing the film at 350$^\circ$C.[266] They also investigated the electrical properties of alkyl monolayers versus varying chain lengths (1.9–2.6 nm) and found suppressed leakage current densities and low conductivities ($\mu$ < $10^{11}$ cm$^2$ V$^{-1}$ s$^{-1}$) for well-ordered SAMs, and much larger conductivities in deliberately disordered SAMs.[182] One of the first attempts utilizing SAMs of alkylsilanes with a –COOH end group as the gate insulator in a p-type (sexithiophene, 6T) OTFT was demonstrated with respectable performance metrics ($\mu$ = $3.6 > 10^4$ cm$^2$ V$^{-1}$ s$^{-1}$, $I_{on}/I_{off}$ ratio $> 10^{11}$, and $V_T$ = 1.3 $V$).[267] However, TFTs with an aromatic terminated alkyllsiline, 18-phenyloctodecyltrichlorosilane (Ph-O-OTS),

Table 2. Summary of the capacitance $C$ [nF cm$^{-2}$], dielectric constant $\varepsilon_{\text{rel}}$, and OTFT characteristics (gate voltage $V_G$, $\mu$ [cm$^2$ V$^{-1}$ s$^{-1}$], current on/off ratio $I_{on}/I_{off}$, threshold voltage $V_T$ [V], and subthreshold slope SS [mV decade$^{-1}$]) for various SAM and SAMT gate dielectrics.

<table>
<thead>
<tr>
<th>Reference</th>
<th>SAM</th>
<th>$C$ [nF cm$^{-2}$]</th>
<th>$\varepsilon_{\text{rel}}$</th>
<th>$V_G$ [V]</th>
<th>$\mu$ [cm$^2$ V$^{-1}$ s$^{-1}$]</th>
<th>$I_{on}/I_{off}$</th>
<th>$V_T$ [V]</th>
<th>SS [mV decade$^{-1}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[260]</td>
<td>SiCl$_2$(CH$_2$)$_2$COOH</td>
<td>6T</td>
<td>$-$2</td>
<td>3.6 &gt; 10$^4$ ($10^6$)</td>
<td>$10^5$ ($10^7$)</td>
<td>$1.3 &gt; 10^3$ ($10^5$)</td>
<td>$10^4$ ($10^6$)</td>
<td>$10^3$ ($10^5$)</td>
</tr>
<tr>
<td>[271]</td>
<td>PhO-OTS</td>
<td>6T</td>
<td>$-$1</td>
<td>0.04 ($8 &gt; 10^2$)</td>
<td>0.02 ($7 &gt; 10^2$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
</tr>
<tr>
<td>[272]</td>
<td>v-SAND I</td>
<td>710</td>
<td>$-$1</td>
<td>0.06 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[273]</td>
<td>v-SAND II</td>
<td>390</td>
<td>$-$1</td>
<td>1.9 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[274]</td>
<td>7-OTS/Ti SAMT</td>
<td>P5</td>
<td>$-$1</td>
<td>1.3 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[275]</td>
<td>ODPA + Al$_2$O$_3$ (3.6 nm)</td>
<td>700</td>
<td>$-$3</td>
<td>0.6 ($10^2$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[276]</td>
<td>ODPA + HfO$_2$ (3.1 nm)</td>
<td>580</td>
<td>$-$1.5</td>
<td>0.15 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[277]</td>
<td>$\sigma$-PA1 + HfO$_2$ (3.1 nm)</td>
<td>690</td>
<td>$-$1.5</td>
<td>0.22 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
<tr>
<td>[278]</td>
<td>$\sigma$-PA2 + HfO$_2$ (3.1 nm)</td>
<td>640</td>
<td>$-$1.5</td>
<td>0.15 ($10^3$)</td>
<td>$10^3$ ($10^5$)</td>
<td>$10^2$ ($10^4$)</td>
<td>$10^1$ ($10^3$)</td>
<td>$10^0$ ($10^2$)</td>
</tr>
</tbody>
</table>
SAM gate dielectric were investigated by a different group, and drastically enhanced P5 TFT performance was reported.\textsuperscript{[139]} Operating at 2 V, the devices exhibited \( \mu = 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), a very high on/off ratio of \( \sim 10^6 \), \( V_T \sim -1.3 \text{ V} \), and a subthreshold slope of 100 mV decade\(^{-1}\). The OTS-OPh SAM is tightly-packed due to intra-SAM \( \pi-\pi \) interactions and exhibits very low leakage currents \((\sim 8 \times 10^{-7} \text{ A cm}^{-2} \text{ at } 2.5 \text{ V})\), large breakdown fields and capacitances of \( \sim 14 \text{ MV cm}^{-1} \) and \( 900 \text{ nF cm}^{-2} \), respectively.

The Northwestern group investigated SAMs (i.e., SAND types I, II, and III described in Section 2.4.1, Fig. 4) as gate dielectric materials. SANDs were established as excellent insulators via solution-phase cyclic voltammetry and MIS leakage current measurements (current densities in the range of \( 10^{-8} \text{ to } 10^{-7} \text{ A cm}^{-2} \)), where measured breakdown fields for I–III were \( \sim 5 \text{–} 7 \text{ MV cm}^{-1} \).\textsuperscript{[135]} Capacitance–voltage (C–V) measurements on MIS structures reveal maximum capacitances \( C_0 = 400 \text{ (I)}; 710 \text{ (II)}; 390 \text{ (III) nF cm}^{-2} \) at 10\(^5\) Hz. It was found that annealing at 120–180 °C reduces C–V hysteresis width to 0.1 V and reduces frequency-dependent C–V dispersion, suggesting that pristine I–III contain quantities of fixed positive charge densities \( Q_1 \), \( 2 \times 10^{12} \text{–} 5 \times 10^{12} \text{ cm}^{-2} \).\textsuperscript{[256,268]} Interface state densities \( D \) calculated from capacitance–voltage (C–V) plots were \( 3 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2} \), and it was found that annealing (120–180 °C) reduces \( Q_1 \) and \( D \) to \( 10^{13} \text{ cm}^{-2} \) and \( 10^{13} \text{ eV}^{-1} \text{ cm}^{-2} \), respectively. Various oligothiophene semiconductors and n-type CuPc TFTs were fabricated with SANDs as the gate dielectrics, and comparable mobilities were measured to those obtained on 300 nm SiO\(_2\), but at much lower operating voltages for the devices with SAND gate dielectrics. It was noted that TFT performance could be improved by patterning the gate electrode, or by incorporating higher-\( k \) molecules in the SAND gate dielectric.

To enhance the TFT performance of SAND gated TFTs, a new self-assembly procedure for the fabrication of multilayer SAND-like gate dielectrics via room temperature vapor phase deposition (v-SAND, Fig. 18) was demonstrated.\textsuperscript{[269]} In addition, the structures of the new molecular constituents (1 and 2) are improved over the original molecular component (Sb) of SANDs by (i) their ability to self-assemble via head-to-tail intra-molecular hydrogen-bonds, and (ii) anticipated larger molecular polarizabilities than Sb. Here, the trends in dielectric permittivities are evaluated qualitatively using the Clausius–Mossotti relation \( \varepsilon \propto (3 + 2\alpha N)/(3 - \alpha N) \) (where \( \alpha \) is the polarizability along the conjugated long axis of the molecule and \( N \) is the molecular density in \( \text{cm}^{-3} \)) in conjunction with sum-over-states\textsuperscript{[270]} calculated molecular polarizabilities. Uniform films (rms roughness\(<1 \text{ nm} \) on native SiO\(_2\) were measured to be 3.5 nm thick by X-ray reflectivity.\textsuperscript{[271]} Additionally, a process for the room temperature, vapor-phase deposition of an SiO\(_2\) Cap layer (similar to step (ii) Fig. 4) was developed. Here, the capping layer thickness on the SAMs is 5.5 nm for a 20 min exposure to Si\(_2\)O\(_5\)Cl\(_2\) vapor. Low leakage current densities \((\sim 10^{-8} \text{ A cm}^{-2} \text{ and large capacitances (400 nF cm}^{-2} \text{) at } 2 \text{ V were measured in MIS devices. Back calculation of the molecular } k \text{ using the parallel plate model for three capacitors in series reveals high-} \kappa \text{s of } 11 \text{ and } 9 \text{ for } 1 \text{ and } 2, \text{ respectively. Interestingly, P5 TFTs fabricated with v-SANDs have very large mobilities (2–3 cm}^2 \text{ V}^{-1} \text{ s}^{-1} \text{ and } I_{PD} \text{ and } I_{OFF} \text{ ratios (} \sim 10^4 \text{), achieving the goal of optimizing TFT performance. Since the dielectric-semiconductor interface is essentially the same for solution processed SAND and v-SAND based P5 TFTs, the performance enhancement can be rationalized by: (i) increased polarizability of the molecular layers 1 and 2 versus the Sb molecular layer used in SAND, and (ii) favorable P5 growth morphology on top of v-SANDs, which exhibits large grains of the P5 in the “thin film” phase\textsuperscript{[39]} by XRD characterization. Zuppiroli et.al. claimed that vapor deposition leads to better electrical performance than solution-based methods.\textsuperscript{[272]} In this example of vapor-phase gate dielectric OTFTs, fabrication begins with an Al\(_2\)O\(_3\) adhesion layer (6 nm) deposited on top of the SiO\(_2\) substrate, followed by deposition of either anthracene-9-carboxy acid (anthracene-COOH), or phenylundecanoic acid (see Fig. 19A for molecular structures), and only 10 nm of P5 for the active channel. Enhanced P5 mobilities were observed in devices with phenylundecanoic acid gate dielectrics compared to bare SiO\(_2\) gate dielectrics, although both P5 films had similar grain sizes. Since it is known that silanol groups give rise to surface traps in SiO\(_2\) dielectrics, the authors claimed that charge transfer from the PE to trap sites of the bare SiO\(_2\) surface generates residual charge carriers at the semiconductor-dielectric interface. Four-probe conductivity measurements were used to quantify the density of these residual charge carriers, \( \rho = \sigma_{PP}(\mu_e) \), where \( e \) is the charge of the electron. For SiO\(_2\) (with the most surface defects), \( \rho = 1.0 \times 10^{13} \text{ cm}^{-2} \), for the anthracene-COOH SAM \( \rho = 1.3 \times 10^{13} \text{ cm}^{-2} \), and for the phenylundecanoic acid SAM, the charge density is the smallest \( \rho = 1.4 \times 10^{11} \text{ cm}^{-2} \).
Recently, hybrid inorganic/phosphoric acid SAMs were used as gate dielectrics in low-voltage OTFTs. In this contribution, phosphoric acid (PA) SAMs deposited on SiO$_2$ (1.7 nm)/HfO$_2$ (3.1 nm thick) substrates were used as the gate dielectric in P5 TFTs. Phosphoric acid SAMs were used because of their better stability to moisture and less homocondensation during device fabrication compared to their silane-based counterparts. The SAM molecular structures investigated in this study (Fig. 19B) combine the advantages of phosphoric acid SAMs previously (such as PhO-OTS, and anthracene-COOH) by incorporating a long insulating carbon chain with a polarizable terminal group in both (2-anthryl)undecoxycarbonyl-phosphonic acid (π-PA1) and (2-anthryl)undecoxycarbonyl-phosphonic acid (π-PA2). The hybrid HfO$_2$/PA-SAMs exhibit large capacitances of 690 nF cm$^{-2}$ (π-PA1) and 640 nF cm$^{-2}$ (π-PA2) compared to SAMs of n-octadecylphosphonic acid (ODPA, 580 nF cm$^{-2}$), and low leakage current densities of $10^{-8}$ to $10^{-9}$ A cm$^{-2}$ at 2 V, allowing for a P5 TFT operating voltage of only $-1.5$ V. Improvements in the P5 TFT performance such as larger mobilities, enhanced $I_{on}$/I$_{off}$ ratios, and lower subthreshold slopes ($-100$ mV decade$^{-1}$) were observed for the π-PA-based OTFTs compared to the bare HfO$_2$ control devices, and were explained by a combination of surface energy and chemical functionality at the P5/dielectric interface.

In another example of hybrid organic/inorganic gate dielectrics, rapid vapor-phase fabrication techniques were used to build superlattices of alkene-terminated SAMs with TiOH interlayers. The hybrid SAMs were formed by exposing TiO$_2$-coated Si substrates to 7-octenyltrichlorosilane (7-OTS) in the presence of H$_2$O vapor at temperatures of 100 and 20 °C. The terminal SAM vinyl groups were converted to carboxylic groups with ozone treatment in the ALD (atomic layer deposition) growth chamber. SAMTs were then built up by generating an active titanium hydride layer on the COOH-terminated SAM by vapor phase titanium isopropoxide adsorption, followed by an exchange reaction with water. SAMT films were fabricated by repetition of these three steps (Fig. 19C). Leakage current density versus voltage characteristics of the Pt/multilayer SAM/Pt capacitors were measured for SAM thicknesses from 1.1–99 nm (Fig. 19C). P5 TFTs using the 100 nm-thick multilayer SAMs (further treated with a hydrophobic SAM as a surface treatment), exhibit $\mu = 1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, at operating voltage of only $-1$ V (due to high dielectric constant of the SAM = 17), $I_{on}$/I$_{off}$ current ratio >500, and $V_T = -0.48$ V. Furthermore, the authors demonstrated two-terminal electrical bistable devices, which can be switched on and off reproducibly more than $10^9$ times due to charge filling and defilling of the defects in the TiO$_2$ layer or interfacial layers.

Similarly, the effects of multilayers of SAND type III (named III-n, where n indicates the number of repeating SAND III units, typically n = 3, and d ~16 nm) as the gate dielectric in TFTs have been intensely investigated. SAND robustness studies were begun by first demonstrating the compatibility of III-3 with carbon nanotube semiconductors for low voltage TFTs. Here the SAND multilayers (~16 nm thick) were deposited conventionally from the solution phase, and have a measured capacitance of 170 nF cm$^{-2}$. Single-wall carbon nanotubes (SWCNTs) were grown by CVD onto SiO$_2$/Si wafers and then transfer printed directly onto the SAND dielectric. The resulting film has ~10 tubes μm$^{-2}$ which act as the semiconducting film in the TFTs. Good SWNT-SAND adhesion allows direct photolithographic patterning of the source and drain electrodes by lift-off. TFT performance is greatly improved over control devices using 100 nm SiO$_2$ gate dielectrics as indicated by substantially lowered hysteresis and $V_T$ shifts. Since the SiO$_2$ control and SAND have very similar surface properties (such as the number of fixed charges, interface state densities, and surface chemistry), the enhanced properties of the TFTs were attributed principally to reduced operating voltage, which avoids charge injection traps arising from adsorbed water near/on the SWCNTs at high voltages. TFT performance is excellent with $\mu$ ~5.6 cm$^2$ V$^{-1}$ s$^{-1}$ in the linear regime, $V_T = 0.2$ V, and a low gate leakage current of ~10 nA at $V_C = -1$ V. In addition, compatibility with n-type SWCNTs (by
PEI coating) was demonstrated by the small observed hysteresis and measured TFT properties: \( \mu = 4.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) and \( V_T = -0.2 \text{ V} \) for applications in low voltage complementary logic gates. Significant gains (\(-8 \times\)) were measured, which were the highest at the time compared to 100 nm SiO\(_2\) gate dielectrics.\[^{[273]}\]

High-performance single carbon nanotube field effect transistors with a thin gate dielectric based on a SAM gate dielectric of PhO-OTS\[^{[29]}\] (2 nm thick) were demonstrated by Klauk et al.\[^{[276]}\]. This is the first systematic study of the stability of a SAM to various e-beam exposures. The authors find negligible change in leakage current density compared to evaporated Au metal contacts when using an electron dose of 300 \( \mu \text{C cm}^{-2} \). However, leakage current increases to \( >10^{-6} \text{ A cm}^{-2} \) at doses larger than 1800 \( \mu \text{C cm}^{-2} \). Operating under ambient conditions, the TFTs exhibited large transconductance (20 \( \Omega \text{cm}^2 \) S), small hysteresis, and a low subthreshold slope (60 mV decade\(^{-1}\)) from which the authors estimate a low interface state density (\( N_s \approx 10^{10} \text{ cm}^{-2} \text{ eV}^{-1} \)). Thin films of In\(_2\)O\(_3\) (60 nm on III-\(\text{Si}\), and 120 nm on 300 nm SiO\(_2\)) were deposited at room temperature by ion-assisted deposition (IAD) directly on top of the dielectric (note that SAND is stable to the in situ ion/plasma exposure during In\(_2\)O\(_3\) growth). The conductivities of the thin films were measured to be \( 10^{-5} \sim 10^{-2} \Omega \text{ cm} \), and XRD revealed substantial crystallinity on both SiO\(_2\) and SAND growth surfaces. Significant In\(_2\)O\(_3\) TFT performance enhancement is observed with SAND-gated devices, where \( \mu = 140 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), interfacial trap density \( D = 10^{11} \text{ cm}^{-2} \text{ V}^{-1} \), \( V_T = 0.0 \text{ V} \) with nearly hysteretic free response, on/off = \( 10^5 \), and the subthreshold slope = 150 mV decade\(^{-1}\), compared to the performance on SiO\(_2\)-gated devices, where \( \mu = 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), on/off = \( 10^5 \). To correct for the performance differences arising from the different dielectric layers, the TFT transfer currents versus charge carrier density are evaluated. It is found that SAND-based devices turn on at much lower accumulated charge carrier densities than SiO\(_2\), indicating greater charge injection efficiency in the former than the latter. To realize fully transparent TFTs, the same fabrication procedures were followed except utilizing glass/ITO as the bottom gate electrode and In\(_2\)O\(_3\) source and drain electrodes. The performance of SAND-based transparent TFTs is the same as on n\(^+\)-Si substrates with an improved subthreshold slope = 90 mV decade\(^{-1}\). These materials combinations advance the field toward the realization of plastic electronic displays featuring optical transparency, mechanical ruggedness, environmental stability, and inexpensive/large area fabrication.

In further work, it was demonstrated that the power consumption efficiency (which is the main technical challenge in the development of truly viable flexible displays) of single ZnO NW (nanowire)-based TFTs is enhanced by the use of SAND type III-\(\text{Si}\) (16 nm) as the gate dielectric (Fig. 20A).\[^{[278]}\] ZnO nanowires (80 nm average diameter, and 5 \( \mu \text{m} \) average length) were purchased from Nanolab Inc. The NWs were dispersed in 2-propanol and the dispersions were transferred to the SAND-coated Si substrates. Source and drain Al electrodes were deposited by electron beam evaporation and patterned by photolithography and lift-off. The SAND dielectrics were first electrically characterized in MIS devices (Al/SAND/Si), and a leakage current density \( \sim 10^{-8} \text{ A cm}^{-2} \) and a capacitance of 180 nF cm\(^{-2}\) at 1 V were measured, verifying the compatibility

---

**Figure 20.** A) Field-emission SEM image of a 130 nm diameter ZnO-NW TFT (the scale bar is 2 \( \mu \text{m} \)) (top), and TFT output characteristics for a SAND-based ZnO-NW TFT (middle), and TFT using 70 nm SiO\(_2\) as the gate dielectric (bottom). Reprinted with permission from [278]. Copyright 2005, American Chemical Society. B) TFT transfer characteristics for varying proton radiation doses of ZnO-NW TFTs with SiO\(_2\) (top) and SAND gate dielectrics (bottom). Reprinted with permission from [279]. Copyright 2006, American Institute of Physics.
of SAND with photolithography and e-beam evaporation methodologies. SAND-gated ZnO NW-TFTs showed reduced operating voltages from 2.5 V to <1.5 V, while maintaining the device on/off ratio and increasing the on-current to 2 μA (from 0.3 μA on SiO₂). The Vᵦ of SAND-gated ZnO NW-FETs was first observed to be ~0.4 V (possibly due to the native SiO₂ and inherent fixed charge in the SAND), and the subthreshold slope was 400 mV decade⁻¹, suggesting some surface traps. Therefore, SAND-based ZnO NW-TFTs were treated with shielded ozone exposures, and the subthreshold slope was reduced to 150 mV decade⁻¹. In addition, reduced Vᵦ (0.2 V) and improved I₉₀/İ₀ff ratios (10⁸) were observed. This performance enhancement is attributed to the NW doping density, and an improved NW-SAND interface. The calculated mobility (taking into account the cylindrical geometry of the channel), is 196 cm² V⁻¹ s⁻¹, which is much greater than 8–18 cm² V⁻¹ s⁻¹ measured for ZnO NW on thick SiO₂ dielectrics, and 54 cm² V⁻¹ s⁻¹ on the control SiO₂ (70 nm thick). The mobility varies from 164–181 cm² V⁻¹ s⁻¹ with varying NW diameter and length.

To examine the radiation stability of SANDs, proton radiation (10 MeV H⁺) hardness testing of these single ZnO-NW SAND gated TFTs was conducted. The radiation tolerance was investigated for space-based applications, and after various dosing and exposure conditions, the Vᵦ of the TFTs did not shift significantly (Fig. 20B). SAND gated TFTs recently went to the International Space Station on the Endeavor space shuttle for further radiation testing. These results suggest that the bulk oxide trap density and interface trap density formed in SAND (or at the SAND-ZnO NW interface) during H⁺ irradiation are significantly lower than traditional SiO₂ gate dielectrics, thus prompting the interface studies of ZnO-NW TFTs using low-frequency noise and temperature-dependent I–V measurements.

The technique of low-frequency noise measurements was used to quantify the surface/interface states in the ZnO-NW TFTs. For SAND gated ZnO-NW, the current noise amplitude increases with increasing V₄₀ bias (Fig. 21A). The authors quantify the interface trap densities by applying Hooge’s empirical model of 1/f noise behavior to the SAND-based devices and to the SiO₂-based control devices. Lower 1/f noise constants are found for SAND-based devices, and the authors conclude that the interface trap densities are comparable to those for the aforementioned SWCNT devices ($D \sim 10^{11} \text{cm}^{-2} \text{V}^{-1} \text{s}^{-1}$) by comparison of Hooge’s constants. Larger temperature variation of the transfer curves, and larger threshold voltage shifts (ΔV₄) versus temperature are observed for the SiO₂/ZnO-NW TFTs compared to the SAND gated devices, and provide further evidence that the SAND/ZnO-NW TFTs have low interface trap and defect densities. Also, temperature-dependent leakage current densities were collected over 25–100 °C (Fig. 20B), and the data analyzed in three regions: (i) thermal generation, (ii) subthreshold region, and (iii) on-state region. For SAND/ZnO NW-TFTs, the maximum activation energy of 0.36 eV is measured at V₄₀ < ~0.65 V, which is just below the Vᵦ. It is found that increasing the positive bias above the Vᵦ decreases the barrier to electron injection, which corresponds to the smaller activation energies measured above Vᵦ (0.05–0.1 eV) and the role of the contact resistance on the TFT performance.

From the foregoing results it is clear that SANDs are robust and compatible with a wide range of inorganic semiconductors (Table 3). However, the successful implementation of any organic dielectric material with a solution-processed inorganic semiconductor layer in a TFT had not been achieved until recently, when it was demonstrated that SAND-based TFTs could be fabricated with solution-processed cadmium selenide (CdSe).

Table 3. Summary of the capacitance $C$ [nF cm⁻²] and TFT characteristics (gate voltage $V₃$ [V] and source/drain voltage $V₄$ [V], μ [cm² V⁻¹ s⁻¹], current on/ off ratio $I₉₀/I₄₀$, threshold voltage $V₄$ [V], and subthreshold slope SS [mV decade⁻¹]) for various SAND gate dielectrics with inorganic semiconductors (ISC).

<table>
<thead>
<tr>
<th>Reference</th>
<th>SAM</th>
<th>$C$ [nF cm⁻²]</th>
<th>ISC</th>
<th>$V₃$ [V]</th>
<th>$V₄$ [V]</th>
<th>μ [cm² V⁻¹ s⁻¹]</th>
<th>$I₉₀/I₄₀$</th>
<th>$V₄$ [SS]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[275]</td>
<td>PhO-OCTS + SiO₂ (4 nm)</td>
<td>500 (3.3)</td>
<td>SWCNT</td>
<td>−1 (−1)</td>
<td>5.6 (10⁵)</td>
<td>−0.2 (60)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[274]</td>
<td>SAND III-3</td>
<td>170</td>
<td>p-SWCNT</td>
<td>−1 (−1.5)</td>
<td>5.6</td>
<td>0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SAND III-3</td>
<td>170</td>
<td>n-SWCNT (PEI coating)</td>
<td>1 (1)</td>
<td>4.1</td>
<td>−0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[276]</td>
<td>SAND III-3</td>
<td>180</td>
<td>In₂O₃</td>
<td>1 (1)</td>
<td>140 (10⁵)</td>
<td>0.33 (150)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[277]</td>
<td>SAND III-3</td>
<td>180 (3)</td>
<td>ZnO NW</td>
<td>1.5 (0.1)</td>
<td>~196 (~10⁵)</td>
<td>0.2 (150)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[276]</td>
<td>SAND III-3 (400 °C annealed)</td>
<td>274</td>
<td>CdSe</td>
<td>4 (2)</td>
<td>41 (10⁵)</td>
<td>2.5 (260)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[287]</td>
<td>SAND III-4</td>
<td>180 (5)</td>
<td>In₂O₃ NW</td>
<td>3 (0.1)</td>
<td>258 (10⁵)</td>
<td>0.1 (250)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 21. A) Current noise spectrum of a SAND-based ZnO-NW TFT, and B) temperature-dependent transfer plots for SiO₂/ZnO-NW TFT (left) and SAND/ZnO-NW TFT (right). Reprinted with permission from [281]. Copyright 2008, American Institute of Physics.
as the semiconducting layer. The chemical bath deposition method (employing Cd\(^{+2}\) and sodium selenosulfate, SeSO\(_2\)^{−}\) solutions) was used to deposit the CdSe films on SAND III-3 as the gate dielectric. MIS and TFT characteristics were compared as a function of annealing. It was found that for unannealed, and for 300°C and 400°C annealed SAND samples, the leakage current density remains low \(\sim 1.1 \mu\)A cm\(^{-2}\) at 4 V, but the capacitance increases with increasing annealing temperatures [160 nF cm\(^{-2}\) (unannealed) < 225 nF cm\(^{-2}\) (300°C) < 274 nF cm\(^{-2}\) (400°C)], which is most likely due to sharper \(\sigma\tau\) organic/Cap interfaces and film reconstructive morphology changes (e.g., thermal condensation of residual Si–OH groups). The maximum performance \((I_{\text{on}}/I_{\text{off}}\) ratio = 10\(^6\), \(V_T = 3.0\) V, and subthreshold slope = 0.26 V decade\(^{-1}\)) was found for CdSe SAND-based TFTs annealed at 400°C. Considering the results of alkoxysilane annealing\(^{[209]}\) and SiO\(_2\) trapping\(^{[210]}\), mentioned previously, this result may not be surprising given that there are multiple siloxane Cap layers in the total 16 nm thickness of SAND III-3. In general, it was found that SAND-based CdSe TFTs have larger mobilities \((\mu = 15\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) for 300 and 400°C annealing, respectively) than SiO\(_2\)-based devices \((\mu = 1.3\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) for 300 and 400°C annealing, respectively). The thermal robustness and solution-phase semiconductor deposition compatibility of SANDs make the scope of applications in a wide variety of organic and inorganic electronics much broader.

Thus far the focus has been on the compatibility of SANDs with unconventional semiconductors. However, SANDs are functional on a wide range of substrates. To this end, junction field effect performance enhancement and surface passivation using SANDs (I and III) was compared to that achieved by 1-octadecanethiol (ODT) on GaAs (Fig. 22).

In related work, Klauk et al. demonstrated low operating voltage complementary organic circuits with SAM gate dielectric OTFTs. The ODPA SAM was first characterized in MIS devices to have capacitances of 0.7 \(\mu\)F cm\(^{-2}\) and leakage current densities of \(j < 5 \times 10^{-6}\) A cm\(^{-2}\) (at 3 V). ODPA-based P5 TFTs exhibited \(\mu = 0.4\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), \(I_{\text{on}}/I_{\text{off}}\) current ratio = 10\(^5\), and a subthreshold swing of 100 mV decade\(^{-1}\). Furthermore, the simulations by incorporating negative fixed charges \((Q_p = -1.85 \times 10^{12} \text{ cm}^{-2})\) to the fit data. These charges are attributed to the negative iodide counter ions in the \(\pi\)-conjugated Sb layer, which create a strong local electrical field oriented toward the underlying GaAs surface, indicating that the ionic charges present in SAND III are essential for the enhanced GaAs junction field effect transistor performance.

In related work, Klauk et al. demonstrated low operating voltage complementary organic circuits with SAM gate dielectric OTFTs. The ODPA SAM was first characterized in MIS devices to have capacitances of 0.7 \(\mu\)F cm\(^{-2}\) and leakage current densities of \(j < 5 \times 10^{-6}\) A cm\(^{-2}\) (at 3 V). ODPA-based P5 TFTs exhibited \(\mu = 0.4\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), \(I_{\text{on}}/I_{\text{off}}\) current ratio = 10\(^5\), and a subthreshold swing of 100 mV decade\(^{-1}\). Furthermore, the

---

**Figure 22.** A) GaAs/SAND JFET device structure, and B) transfer characteristics utilizing the indicated gate dielectrics. Reprinted with permission from [282]. Copyright 2008, American Institute of Physics.

**Figure 23.** A) SAM molecular structure and device fabrication schematic. B) Complementary circuits with ODPA based TFTs (for the lowest leakage current deposition procedure). Reprinted with permission from [286]. Copyright 2008, American Chemical Society.
authors demonstrated compatibility of the SAM with an n-type organic semiconductor hexadecafluorocopperphthalocyanine (F16CuPc), and measured performance metrics similar to those reported in the literature. Using these SAMs with P5 and F16CuPc organic semiconductors, low voltage (1.5–3 V) complementary circuits and ring oscillators were demonstrated with a static power consumption of less than 1 nW per logic gate. Expanding on this work, Halik and co-workers next demonstrated micro-contact-printed ODPA SAMs as the gate dielectric for TFTs and complementary circuits on AlOx/Al substrates (Fig. 23).[287] They found that TFTs and complementary circuits fabricated by printing and subsequent wet etching perform identically to the TFTs and ring oscillators reported previously where the gate electrodes were patterned by shadow-masking. Nonetheless, this is the first demonstration of a printing process that uses the direct printing of a SAM layer, and subsequently uses that layer as an etch resist to pattern the bottom gate electrodes.

The insight from the above examples of SAM- and SAMT-based TFTs has enabled one of the most unconventional hybrid organic–inorganic electrical technologies reported to date: transparent active matrix organic light-emitting diode (AMOLED) displays powered by nanowire electronics.[288] This is the first example of transparent AMOLED display elements composed of 54 × 176 μm OLED pixels, in which the switching and driving circuits are comprised exclusively of nanowire transistor (NWT) electronics fabricated at room temperature. Proof of concept green-emitting polymer LEDs with interfacial charge-blocking materials were integrated with a transparent bottom contact electrode. The circuit for a unit pixel consists of one switching electrode. The circuit for a unit pixel consists of one switching and one storage capacitor. The device is composed of multiple layers making up the transistor and the OLED (Fig. 24). Briefly, the fabrication begins with 200 nm thick SiO2 layer deposited by e-beam evaporation on a glass substrate. Next, 100 nm of ITO is deposited by IAD at room temperature, and patterned by photolithography. Next, a 22 nm SAND III multilayer (III-4) is deposited on the patterned ITO gate electrodes via solution self-assembly. Contact holes are patterned as anode openings for the OLED units and as bottom gate electrode contacts for the pixel. Next, a suspension of single crystal In2O3 nanowires is dispersed on the substrate. ITO source/drain electrodes are deposited by IAD and patterned by lift-off. Next, 200 nm of SiO2 is deposited for PLED fabrication and characterization. The mobilities of the present SAND-based In2O3 TFTs (μ ~ 258 cm2 V−1 s−1) are similar to In2O3 NWS on oxide dielectrics (μ ~ 6.9–279.1 cm2 V−1 s−1) and bulk single crystals (μ ~ 160 cm2 V−1 s−1). Minor hysteresis, large Isat currents (6 × 10−6 A at Vc = 2.0 V), and low subthreshold slope (0.35 V decade−1) indicate negligible charge trapping and detrapping in/on the SAND and at the NW-SAND interface. Fully transparent, proof-of-concept 2 mm × 2 mm NW-AMOLED arrays (300 pixels = 900 NWTs) were fabricated using a very thin Al cathode on glass substrates. The optical transmission values are 72% (before OLED deposition- limited by the thin Al cathode) and 35% (after OLED deposition) in the 350–1350 nm wavelength range, which corresponds to a green peak luminescence of >300 cd m−2. Note that transmission coefficients up to 70% have been reported for OLED structures on plastic substrates.[289] This fabrication process involves fewer mask steps than conventional Si approaches and is very promising for future AMOLED displays.

4.4. SAMs as the TFT Semiconductor Channel

As described in Section 4.2, several groups have studied the thickness dependence of mobility for various semiconductors, and for P5 and CuPc the mobilities begin to saturate after 6 monolayers of semiconductor deposition.[290,291] This pheno-

![Figure 24](image-url)
enon opens the possibility of using SAMs and SAMTs as the active channel in TFTs.[286–294] In 2005, Pilkuhn and co-workers studied ODTS SAMs with different end group functionalizations, such as methyl, thiol, thiophene, phenoxy, and biphenyl.[292] Of particular interest were the good insulating properties of the alkyl chain (large breakdown field $E_b = 16$ MV cm$^{-1}$), and the simultaneous lateral (in-plane) conductance of the I$_2$-doped biphenyl end group, suggesting these SAMs could be used as SAM-TFTs. In the same year, Malliaras and co-workers studied the dependence of PS with film thickness, and found that the mobility saturates at ~0.45 cm$^2$ V$^{-1}$ s$^{-1}$ after 6 monolayers.[295] In 2007, Horowitz and co-workers demonstrated with rather complicated device fabrication (e-beam lithography of short channel lengths $<1$ μm), that SAMs of bifunctional silanes on SiO$_2$ (Fig. 25A) could be used as the semiconductor layer in TFTs.[296]

However, for sensing applications mobility saturation starting at only 1–2 monolayers is desirable.[297] In 2005 Dinelli et al. studied the hole mobility in ultra thin films of 6T with a functionalized hydroxy bithiophene (HO6OPT), where the surface hydroxyl groups of HO6OPT serve as receptor sites for the device. TFTs were tested upon exposure to 5 ppm of dimethylmethylphosphonate (DMMP) vapors, and it was found that the mobility of the device decreased significantly when the DMMP vapor was injected into the chamber. However, the TFT mobility could be recovered by flowing N$_2$ or by moderate heating of the device (Fig. 25B).[297] Very recently de Leeuw and co-workers reported on SAM-based TFTs using α-substituted quinquethiophene as the semiconductor core (for long range ππ coupling in the monolayer) spaced from the monochlorosilane surface anchoring group by an undecane aliphatic chain (Fig. 25C).[299] Thermally grown SiO$_2$ was used as the gate dielectric, and the top source/drain electrodes were fabricated by conventional photolithographic methods. The SAM-TFTs exhibited highly reproducible bulk-like hole mobilities (0.04 cm$^2$ V$^{-1}$ s$^{-1}$, 40 μm channel length), and large current modulation. Furthermore, the authors fabricated SAM-based TFT inverters (Fig. 25C) and integrated circuits with performance similar to that of state-of-the-art organic integrated circuits for radio-frequency identification transponders.[299] While a true SAM-TFT has yet to be realized, these examples demonstrate significant advances in the area of ultra-thin OTFTs.

5. Conclusions

It is well established that OTFT semiconductor properties and consequently OTFT device performance are strongly linked to the electrical properties of the gate dielectric. However, the gate dielectric does more than just affect the semiconductor growth morphology. SAMs with different molecular dipole moments on conductive electrodes induce surface potential changes that shift the work function or the electron affinity of the bottom metal or semiconductor electrode, respectively. These energy level shifts influence the transport/injection characteristics of the SAM, affecting both the charge accumulation and conduction in the semiconducting channel of the OTFT.[298] While a definite correlation between SAM surface phenomena and TFT performance is not yet established, it is clear that hybrid and SAND gate dielectrics represent an important advance in both fundamental science, and in device applications for the fabrication of low operating voltage unconventional electronic circuits.[286] This constitutes a major step towards flexible electronics.

Acknowledgements

We thank ONR (N00014-02-1-0090), AFOSR (FA9550-08-1-0331), and the NSF-MRSEC program through the Northwestern Materials Research

Figure 25. A) Output characteristic of a typical Si/Al$_2$O$_3$/Pt/SAM transistor with 20 nm channel length and 5 μm channel width; and chemical structures used in SAMs. (note carboxylic acids were not used in the TFTs due to their instability to the e-beam fabrication procedure.). Reprinted with permission from [295]. Copyright 2005, Wiley-VCH Verlag GmbH. B) The field-effect mobility of 6PTTP6 TFTs at various film thicknesses (left), the inset is the same data on a linear scale. The change of the mobility of the ultra-thin TFT with receptor layer upon exposure to 5 ppm DMMP vapor (right), and chemical structures of semiconductors. Reprinted with permission from [296]. Copyright 2007, Wiley-VCH Verlag GmbH. C) Output characteristics of a SAM-TFT having a channel length and width of 40 and 1000 mm, respectively (left). Static input-output characteristics of SAM-TFT based unipolar inverter (right). Where $V_{in}$ is the input voltage and $V_{sat}$ is the output voltage, $V_s = 0$. The inset shows a diagram of the logic gate and a plot of the measured gain, and the chemical structure self-assembled semiconductor is shown to the right. Reprinted with permission from [299]. Copyright 2008, Macmillan Publishers Ltd.
Center (DMR-0520513) for support of this research. This article is part of a Special Issue on Interfaces in Organic Electronics.

Received: November 6, 2008